User Guide

PC7-FESTIVAL • CompactPCI® PlusIO CPU Card

Intel® XEON® E3 v6 Family Mobile Workstation Processor

Contents

About this Manual

This manual describes the technical aspects of the PC7-FESTIVAL, required for installation and system integration. It is intended for the experienced user only.

Edition History

Ed.	Contents/*Changes*	Author	Date
1	User Manual PC7-FESTIVAL, english, preliminary edition (draft) Text #9349, File: PC7_ug.wpd, Source(s): PC7_pi.wpd, SC5_ug.wpd	ekf/sth	5 March 2021
1.1	Document No. fixed	jj	10 March 2021
2	Removed occurrences of PC6-TANGO. Clarified speed options on PlusIO. Corrected some PlusIO connector references	gn	2021-04-14
3.0	Confused page formatting amended Changes with PCB revision 2022 incorporated (2.5GbE backplane option) Photos added	jj	7 September 2022
4.0	Changes regarding P82-GBE, 'Backplane Resources' added	jj	22 September 2022
4.1	Combinations P01-M12 w. S48-SSD and P82-GBE described	jj	11 October 2022
4.2	Photos with PCZ-NVM 8HP assembly added	jj	18 October 2022
4.3	Added SCL-RHYTHM to the suite of eligible side cards (8HP assembly)	jj	3 November 2022
4.4	High speed backplane signal constraints due to J2 UHM backplane connector obsolescence/replacement more clearly explained	jj	14 December 2022
4.5	Power requirements table updated	jj/mko	4 August 2023
4.6	UEFI & ACPI versions updated	jj/cr	26 September 2023
4.7	Photos added PC7 w. P82-GBE low profile mezzanine module	jj	14 December 2023
4.8	Some photos replaced of 8HP assemblies available w. a larger heatsink	jj	4 April 2024

Note: If an EKF product comes labelled with  this special sign according to ISO 7010 M002, please contact support@ekf.com for availability of additional documentation which may be important for proper usage.

Related Documents

Related Information PC7-FESTIVAL	
PC7-FESTIVAL Home	www.ekf.de/p/pc7/pc7.html
PC7-FESTIVAL Product Information	www.ekf.de/p/pc7/pc7.html#PI

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- XEON ®, Core™: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows: ® Microsoft
- EKF, ekf system: ® EKF

Note: EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	Document	Origin
PlusIO	CompactPCI PlusIO Specification, PICMG® 2.30	www.picmg.org
DisplayPort	VESA DisplayPort Standard Version 1.2, DisplayPort Alt Mode on USB Type-C	www.vesa.org
Ethernet	IEEE Std 802.3 IEEE Std 1588-2008 Precision Time Protocol	standards.ieee.org
HD Audio	High Definition Audio Specification	www.intel.com
LPC	Low Pin Count Interface Specification	www.intel.com
M.2	PCI Express M.2 Specification	www.pcisig.com
NVMe	NVM Express specification	www.nvmexpress.org
PCI Express®	PCI Express® Base Specification	www.pcisig.com
SATA	Serial ATA Specification	www.sata-io.org
TPM	Trusted Platform Module 2.0	www.trustedcomputinggroup.org
UEFI	Unified Extensible Firmware Interface UEFI Specification ACPI Specification	www.uefi.org
USB	Universal Serial Bus Specification Type-C Cable and Connector Specification Type-C Locking Connector Specification Universal Serial Bus Power Delivery Specification	www.usb.org

Overview

The PC7-FESTIVAL is a rich featured high performance 4HP/3U CompactPCI® PlusIO CPU board, equipped with an Intel® Xeon® E3 familiy mobile workstation processor for demanding applications. For scalability, the PC7-FESTIVAL is also available with Intel® Core™ processor.

The PC7-FESTIVAL front panel is provided with two RJ45 Gigabit Ethernet jacks, two USB 3.0 Type-A receptacles, and two DisplayPort connectors. In addition, a third USB Type-C front panel receptacle is available as an option, usable alternatively as (third) DisplayPort.

The powerful Xeon® E3-1500 v6 series processor is accompanied by the CM238 mobile PCH, for a maximum of high speed I/O resources (e.g. PCI Express®, SATA, USB).

On-board mass-storage solutions are based on low profile mezzanine expansion cards, which can accommodate up to two M.2 style SSD modules (PCIe® Gen3 x4 and/or SATA 6G). Side cards for an 8HP assembly are also available, providing front I/O and M.2 SSDs.

The PC7-FESTIVAL is equipped with up to 32GB DDR4 RAM with ECC support. Up to 16GB memory-down are provided for rugged applications, and another 16GB are available via the DDR4 ECC SO-DIMM socket.

The backplane connector J1 allows for up to seven CompactPCI® Classic peripheral cards in a system. The J2 connector complies with the CompactPCI® PlusIO standard for high speed rear I/O (fourfold PCIe®, SATA and USB2), or a hybrid CompactPCI® Serial backplane.

Technical Features

Feature Summary

Feature Summary

General

- CompactPCI® PlusIO (PICMG® CPCI 2.30) System Slot Controller
- Form factor single size Eurocard (board dimensions 100 mm x 160 mm)
- Mounting height 3U
- Front panel width 4HP (8HP/12HP assembly with optional mezzanine side card)
- Front panel I/O connectors for typical system configuration (2 x USB3, 2 x DisplayPort, 2 x GbE)
- Backplane communication via CompactPCI® J1 and J2 hard metric connectors
- J1 Connector for PICMG® CompactPCI® Classic 32-Bit support
- J2 Connector (UHM high speed) for CompactPCI® PlusIO support (PCIe®, SATA, USB2) *
- J2 PlusIO configuration allows for either CompactPCI® Serial hybrid backplane usage or rear I/O module attachment
- J2 Connector option available for 64-bit system slot (legacy CompactPCI® 2.0 Classic)
- Side cards and low profile mass storage modules available as COTS and also as custom specific

** In case of obsolescence, the J2 UHM connector will be replaced by the CompactPCI® 2.0 classic J2 connector. This may reduce high speed backplane transfer in particular applications (PCIe Gen1 2.5GT/s, SATA 1.5Gbps). This does not affect peripherals attached via the P-HSE mezzanine connector.*

Power Supply

- +5V, +3.3V according to CompactPCI® 2.0 via J1 backplane connector
- Total power consumption depends on processor type and mezzanine assembly
- +5V only board design for low cost system power supply with all 25W processors *
- SAC (Stand-Alone Computer) option w. two-pos. 5V/10A terminal block (J1/J2 removed)

* option different SKUs available with 25W processors also for +5V/3.3V backplane supply - specify when ordering on request: PC7-FESTIVAL +5V only can deliver +3.3V to backplane for CompactPCI® peripheral boards

Processor

- Intel® Kaby Lake-H mobile platform with ECC (CM238 mobile workstation PCH)

- Intel® Xeon® processor E3 v6 family (mobile workstation)
- Xeon E3 1505L v6 ▪ 2.2/3GHz ▪ 8M ▪ 4C/8T ▪ DDR4 2400 ECC ▪ 25W ▪ GT2 - P630 ▪ vPRO™/AMT
- Xeon E3 1505M v6 ▪ 3/4GHz ▪ 8M ▪ 4C/8T ▪ DDR4 2400 ECC ▪ 45/35W ▪ GT2 - P630 ▪ vPRO™/AMT

- 7th Generation Intel® Core™ mobile processor
- i3 7102E ▪ 2.1GHz ▪ 3M ▪ 2C/4T ▪ DDR4 2400 ECC ▪ 25W ▪ GT2 -630

Feature Summary

Firmware

- Phoenix® UEFI (Unified Extensible Firmware Interface) V2.5 with CSM*
- Phoenix® SCT (SecureCore Technology) Release V4.01
- ACPI V5.0
- Fully customizable by EKF
- Secure Boot and Measured Boot supported - meeting all demands as specified by Microsoft®
- Windows®, Linux and other (RT)OS' supported
- Intel® AMT supported for Intel® Xeon® E3 v6 (disabled by default, must be enabled via BIOS setup)

** CSM (Compatibility Support Module) emulates a legacy BIOS environment, which allows to boot a legacy operating system such as DOS, 32-bit Windows and some RTOS'*

Main Memory

- Integrated memory controller up to 32GB DDR4 2400 +ECC
- DDR4 +ECC soldered memory up to 16GB
- DDR4 +ECC SO-DIMM memory module socket up to 16GB

Mezzanine Mass Storage

- Mezzanine side card connectors for local expansion e.g. SSD mass storage
- Low profile mezzanine modules available (4HP common front panel)
- Side cards available (8HP common F/P assembly)
- P-HSE1 - configurable as 4 x SATA 6G or 4 x PCIe® Gen3 (from CM238 PCH), 1 x USB3
- P-HSE2 - 4 x PCIe® Gen3 (from CM238 PCH) & 3rd DisplayPort (from CPU)
- P-EXP - Legacy interface (from PCH)

- 4HP Low profile mezzanine module options:
- C48-M2 - 2 x M.2 2280 SATA SSD sockets
- S48-SSD - 1 x M.2 2280 NVMe® SSD socket, 1 x M.2 2280 NVMe® or SATA SSD socket (autosense), 1 x Type-C USB F/P connector (enabled for DisplayPort alternate mode)
- P82-GBE - 2 x 2.5GBASE-T for J2 backplane connector, 1 x M.2 2280 NVMe® SSD socket

- 8HP/12HP Mezzanine side card options:
- P01-M12 - Replacement for PC7-FESTIVAL RJ45 GbE jacks by M12-X receptacles
- PCU-UPTEMPO - Side board w. 2 x M.2 SATA SSD sockets & front I/O
- PCZ-NVM - Side board w. 2 x M.2 NVMe® SSD sockets & front I/O
- SCJ-VEENA - M.2 NVMe® or SATA SSD socket (autosense), quad 2.5GBASE-T Ethernet RJ45 jacks
- SCL-RHYTHM - M.2 NVMe® or SATA SSD socket (autosense), quad 1000BASE-T Ethernet M12-X ports

- Custom specific mezzanine side card design - I/O and storage

Feature Summary

Graphics

- Integrated graphics engine, 3 symmetric independent displays
- 3D HW acceleration DirectX12, OpenCL 2.x, OpenGL 4.4, ES 2.0
- HW video decode/encode HEVC10b 10-bit, VP9 10-bit, JPEG
- HDR (High Dynamic Range) Rec. 2020 Wide Color Gamut
- High-bandwidth Digital Content Protection (HDCP)
- UHD premium content playback
- Front panel options: Dual DisplayPort (DP) connectors
- 3rd DisplayPort optional via Type-C connector on low profile mezzanine card
- Max resolution 4096 x 2304 @60Hz (any DisplayPort, concurrent operation)
- DisplayPort™ 1.2 Multi-Stream Transport (MST) - display daisy chaining
- MST max resolution via single DP connector 2880x1800@60Hz (2 displays), 2304x1440@60Hz (3 displays)
- DisplayPort integrated audio (3 independent audio streams)

Networking

- Two networking interface controllers (NIC), 1000BASE-T, 100BASE-TX, 10BASE-T connections
- Port 1 equipped w. I219LM PHY (suitable for Intel® AMT)
- Port 2 equipped w. Intel® I210-IT -40°C to +85°C operating temperature GbE controller
- IPv4/IPv6 checksum offload, 9.5KB Jumbo Frame support, EEE Energy Efficient Ethernet
- IEEE 802.1Qav Audio-Video-Bridging (AVB) enhancements for time-sensitive streams
- IEEE 1588 and 802.1AS packets hardware-based time stamping for high-precision time synchronization
- RJ45 front panel jacks (option 2 x M12-X with mezzanine module P01)
- Option quad 2.5GbE RJ45 front panel ports with SCJ-VEENA side card (8HP front panel width)
- Option quad GbE M12-X front panel ports with SCL-RHYTHM side card (8HP front panel width)
- Option 2 x 2.5GbE over J2 backplane connector with P82-GBE low profile mezzanine module

Chipset

- Intel® CM238 Mobile Workstation Platform Controller Hub (PCH)
- PCIe Gen3 8GT/s
- SATA 6Gbps
- USB3
- GbE
- LPC, Audio, Legacy

Feature Summary

On-Board Building Blocks

- Additional on-board devices, PCIe® based
- PCIe® to PCI® Bridge 32bit 33/66MHz for 7 CompactPCI®Classic peripheral card backplane slots
- 1 x Gigabit Ethernet controller Intel® I210IT (front I/O)
- 1 x Gigabit Ethernet PHY Intel® I219LM (front I/O)
- IEEE 1588-2008 Precision Time Protocol including PPS and PPM signals supported

Security

- Trusted Platform Module
- TPM 2.0 for highest level of certified platform protection
- Infineon Optiga™ SLB 9665 cryptographic processor
- Conforming to TCG 2.0 specificationOption
- fTPM (firmware-based TPM 2.0) or dTPM (discrete TPM) selectable from UEFI (BIOS) setup
- AES hardware acceleration support (Intel® AES-NI)

Front I/O (4HP)

- 2 x Gigabit Ethernet RJ45 (1 = PCH & I219LM - iAMT, 2 = I210IT)
- 2 x DisplayPort (from processor integrated HD graphics engine, standard DP latching receptacles)
- 2 x USB 3.0
- Option 2 x Type-C USB 3.1 Gen1 (requires low profile mezzanine expansion card w. front panel I/O)

Additional Front I/O (8HP)

- Option RS-232, USB3, DisplayPort w. PCZ-NVM side card
- Option quad port 2.5GbE RJ45 jacks w. SCJ-VEENA side card
- Option quad port GbE M12-X receptacles w. SCL-RHYTHM side card
- Option 2 x M12-X receptacles for Gigabit Ethernet (P01, as replacement for RJ45)
- Option RS-232, HD-Audio, USB w. PCU-UPTEMPO side card
- Custom specific front panel and side card design

Feature Summary

CompactPCI® PlusIO Backplane Resources

- PICMG® CompactPCI® 2.0 CPU card & system slot controller for J1 based 32-bit CompactPCI® systems
- Support for up to seven CompactPCI® peripheral boards, 33/66MHz (PI7C9X112 PCIe® to PCI® bridge)

- PICMG® CompactPCI® 2.30 J2 connector pin assignment according to CompactPCI® PlusIO
- J2 is assigned to 4 x PCIe® Gen2*, 4 x SATA 3G*, and 4 x USB2 ports (all derived from PCH)
- Option 2 x 2.5GbE* over J2 backplane connector with P82-GBE low profile mezzanine module
- J2 can be used to enable CompactPCI® Serial peripheral card slots for hybrid systems with a split backplane
- Hybrid small system racks available (e.g. SRP-BLUBOXX)
- J2 can be used alternatively for a rear I/O module
- Custom specific rear I/O module design on request
- J2 Connector option available - 64-bit system slot tolerant for legacy CompactPCI® 2.0 (Classic)
- Gigabit Ethernet 2 x 2.5GBASE-T option w. P82-GBE low profile mezzanine module

** CompactPCI® PlusIO specifies PCIe® 5GT/s, SATA 3G and GbE 1000BASE-T only over J2 UHM. Due to obsolescence of the 3M UHM connector series the PC7-FESTIVAL will be equipped with a standard J2 hard metric backplane connector, which may result in PCIe® 2.5GT/s (Gen1) backplane link training under adverse application conditions.*

Environmental & Regulatory

- Suitable e.g. for industrial, transportation & instrumentation applications
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Long term availability
- Rugged solution
- Coating, sealing, underfilling on request
- Lifetime application support
- RoHS compliant
- Operating temperature 0°C to +70°C
- Operating temperature -40°C to +85°C (industrial temperature range) on request
- Storage temperature -40°C to +85°C, max. gradient 5°C/min
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 11.9 years MIL-HDBK-217F
- EC Regulatory EN55035, EN55032, EN62368-1

Feature Summary

Applications

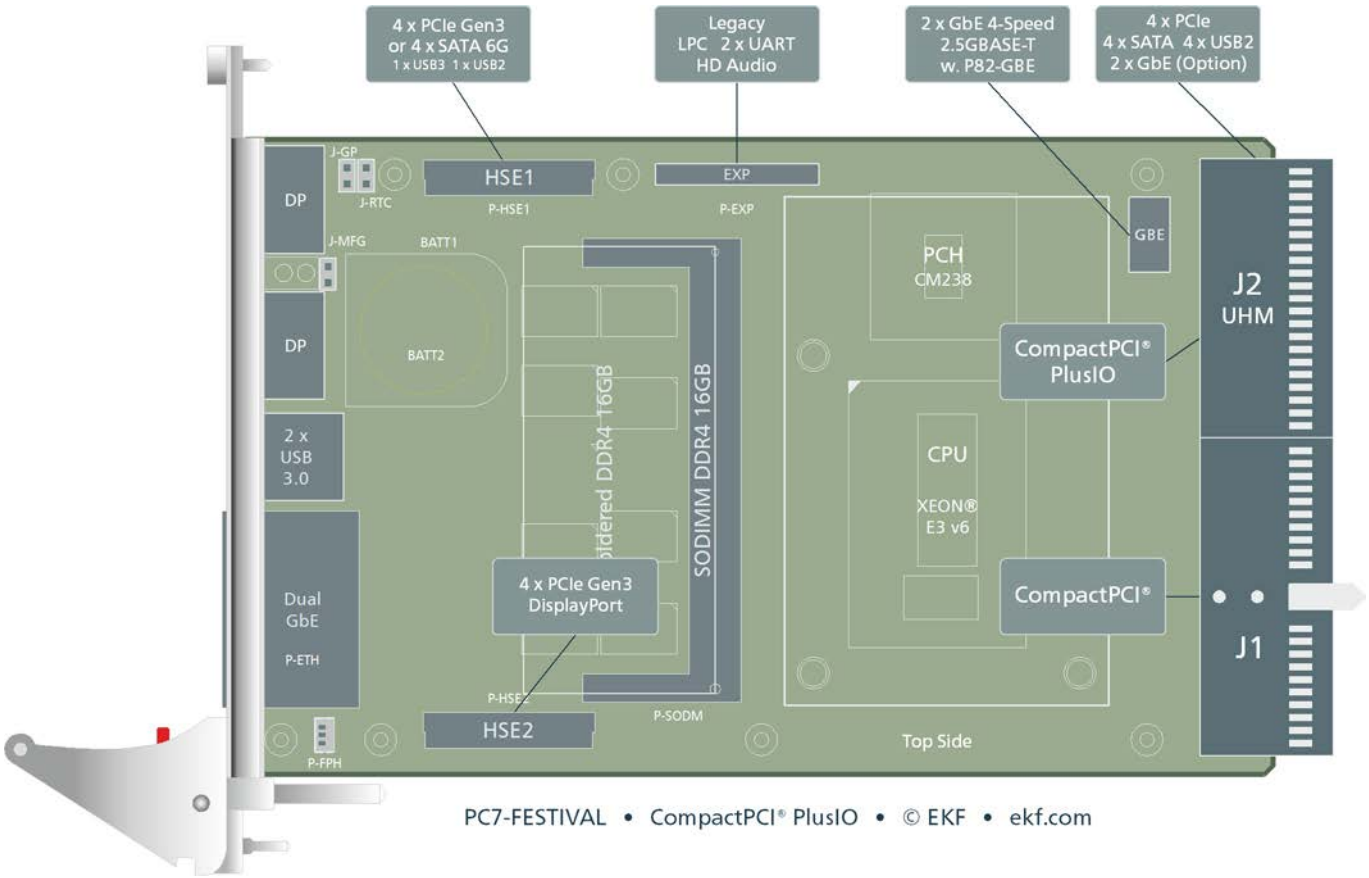
- General industrial computing, for x86 based software
- IIoT applications, edge computing, networking
- Medium to high embedded CPU performance
- CompactPCI® Classic systems upgrade
- CompactPCI® Serial peripheral card expansion
- Stand-Alone Computer (SAC)

Note: Items are subject to changes w/o further notice.

CompactPCI® PlusIO

CompactPCI® PlusIO (PICMG® 2.30) is an enhancement to CompactPCI® Classic which enables system expansion and rear I/O across J2. High speed signal lines (PCI Express®, SATA and USB) are passed from the PC7-FESTIVAL via the J2 connector to the backplane, for usage either with a PlusIO rear I/O transition module, or recent CompactPCI® Serial cards.

CompactPCI® Serial (PICMG® CPCIS.0) defines a card slot based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles CompactPCI® and CompactPCI® Serial can reside, with the PC7-FESTIVAL in the middle as controller for both backplane segments, combining the technologies of both worlds.

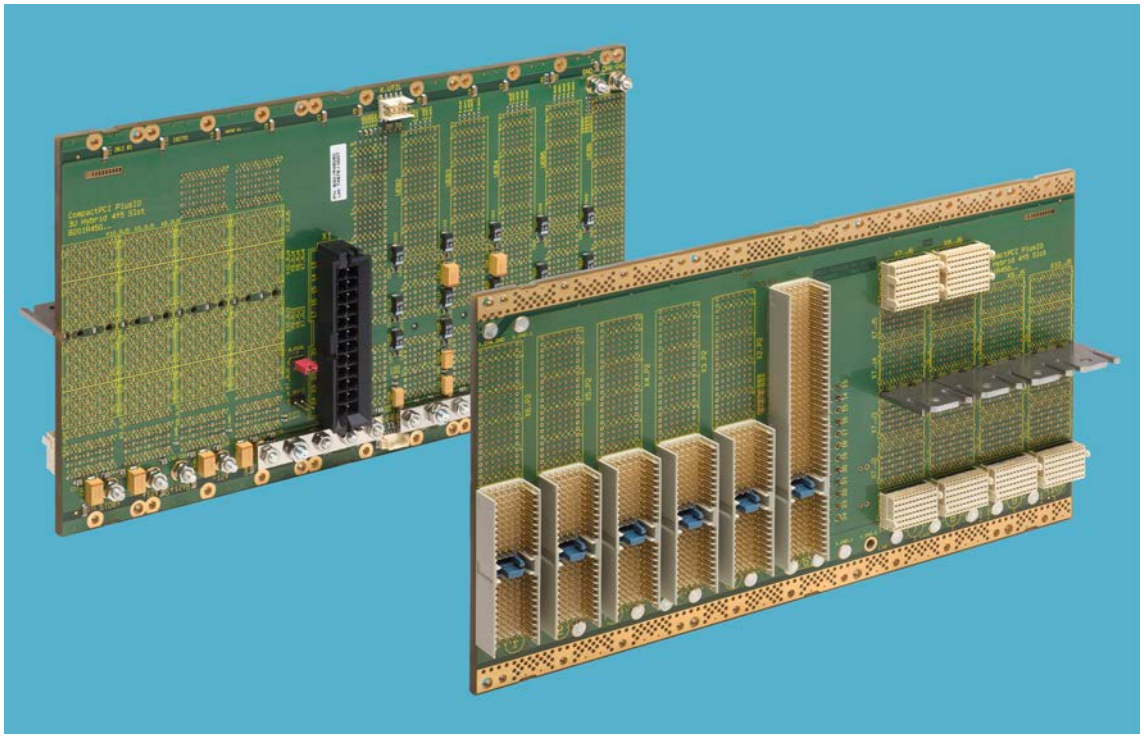


PC7-FESTIVAL • System Expansion Options

New from PCB Rev.2022 off: Expansion Connector GBE for passing 2 x 2.5GBASE-T to J2, as an option with P82 low profile mezzanine module.

Sample CompactPCI® PlusIO Rack

SRP-BLUBOXX



Sample Hybrid Backplane

Sample Hybrid Backplane

Power Requirements

CompactPCI® Board Supply Voltages		
+3.3V +0.17V/-0.1V (+5%/-3%)	+5V +0.25V/-0.15V (+5%/-3%)	+12V -12V not in use

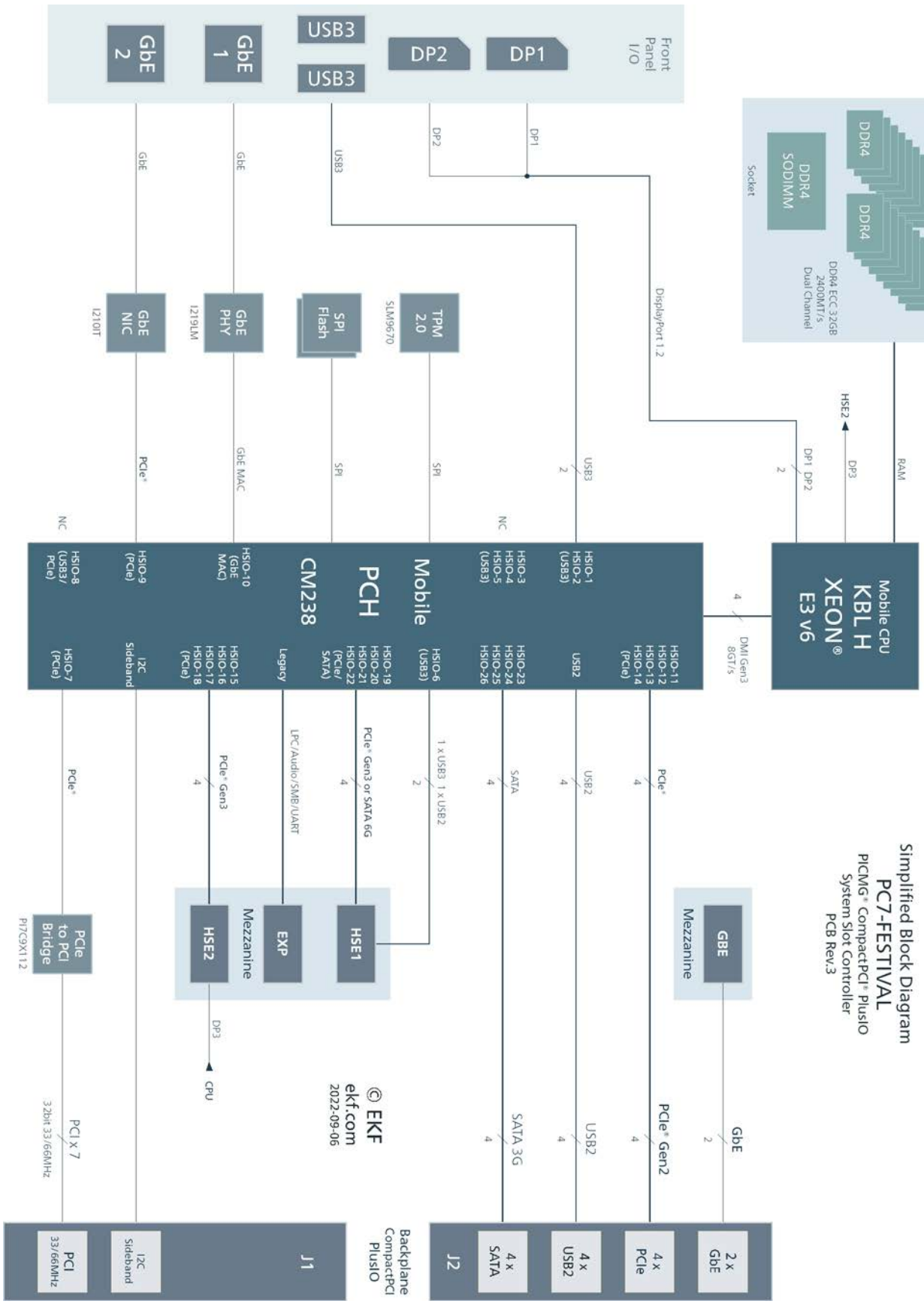
Test Results w. PC7-640D E3-1505m V6 3GHz CPU-ID 0x906e 16GB On-Board RAM PCB Rev.2				
+5V	0.8GHz	2.4GHz	3GHz	3.7GHz
Win10* Idle	1.2A	1.2A	1.2A	1.2A
TAT**: CPU0-7 @50% GFX @70%	4.6A	6.0A	7.5A	11.5A
TAT**: TDP	4.75A	6.1A	10A	12A
TAT**: CPU0 @100%	1.5A	2.3A	2.9A	4.5A
Passmark***	4.6A	6.0A	7.0A	10A
+3.3V	0.8GHz	2.4GHz	3GHz	3.7GHz
Win10* Idle	0.7A	0.7A	0.7A	0.7A
TAT**: CPU0-7 @50% GFX @70%	0.9A	0.91A	0.92A	0.92A
TAT**: TDP	0.9A	0.91A	0.92A	0.92A
TAT**: CPU0 @100%	0.85A	0.86A	0.87A	0.92A
Passmark***	1.3A	1.3A	1.32A	1.33A

* Win10 64bit, Power Plan 'Balanced', external SSD, Ethernet ports not connected

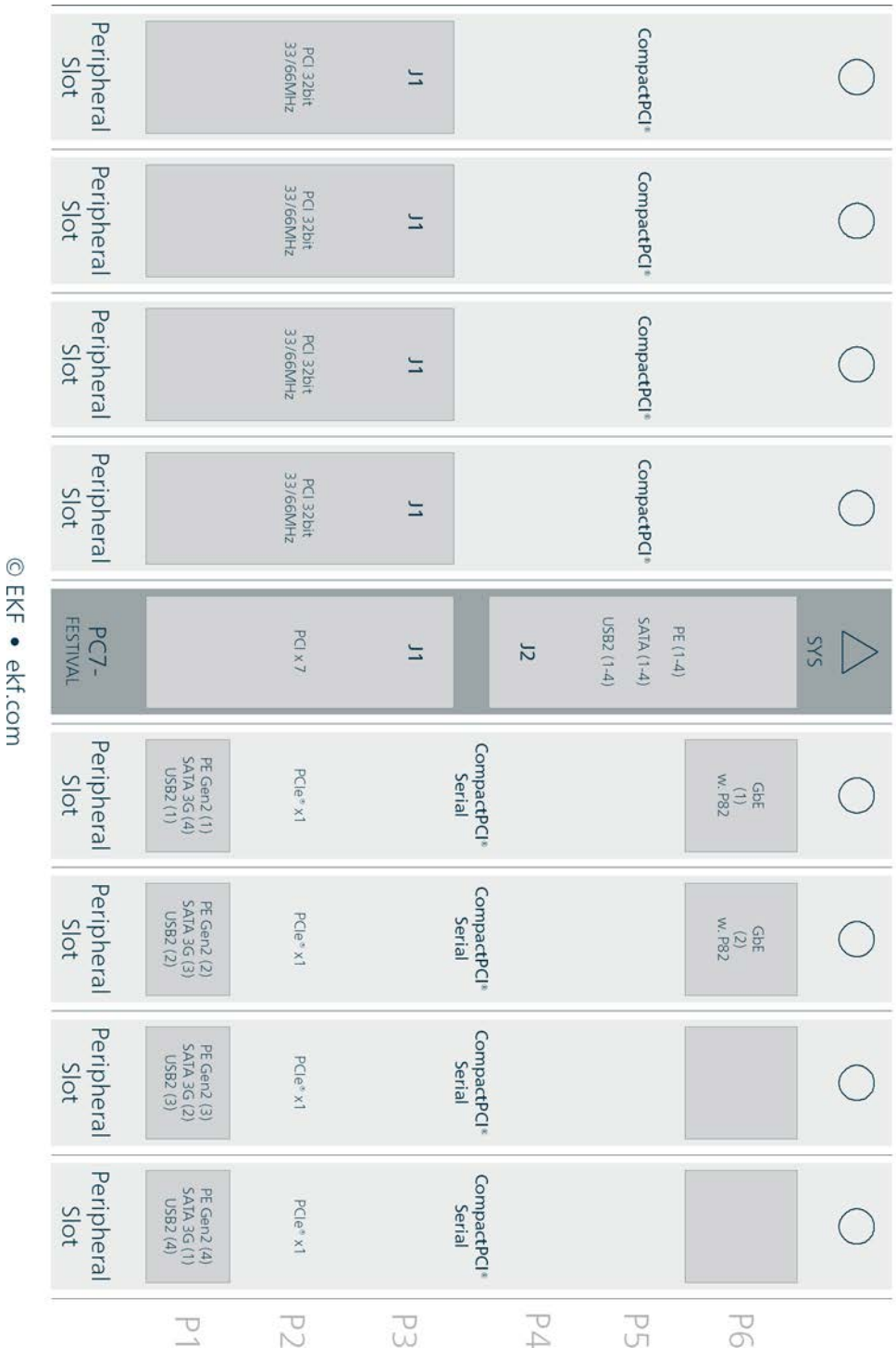
** Intel Thermal Analysis Tool (TAT) Version 6.10.1

*** Passmark BurnInTest V8.1 Pro

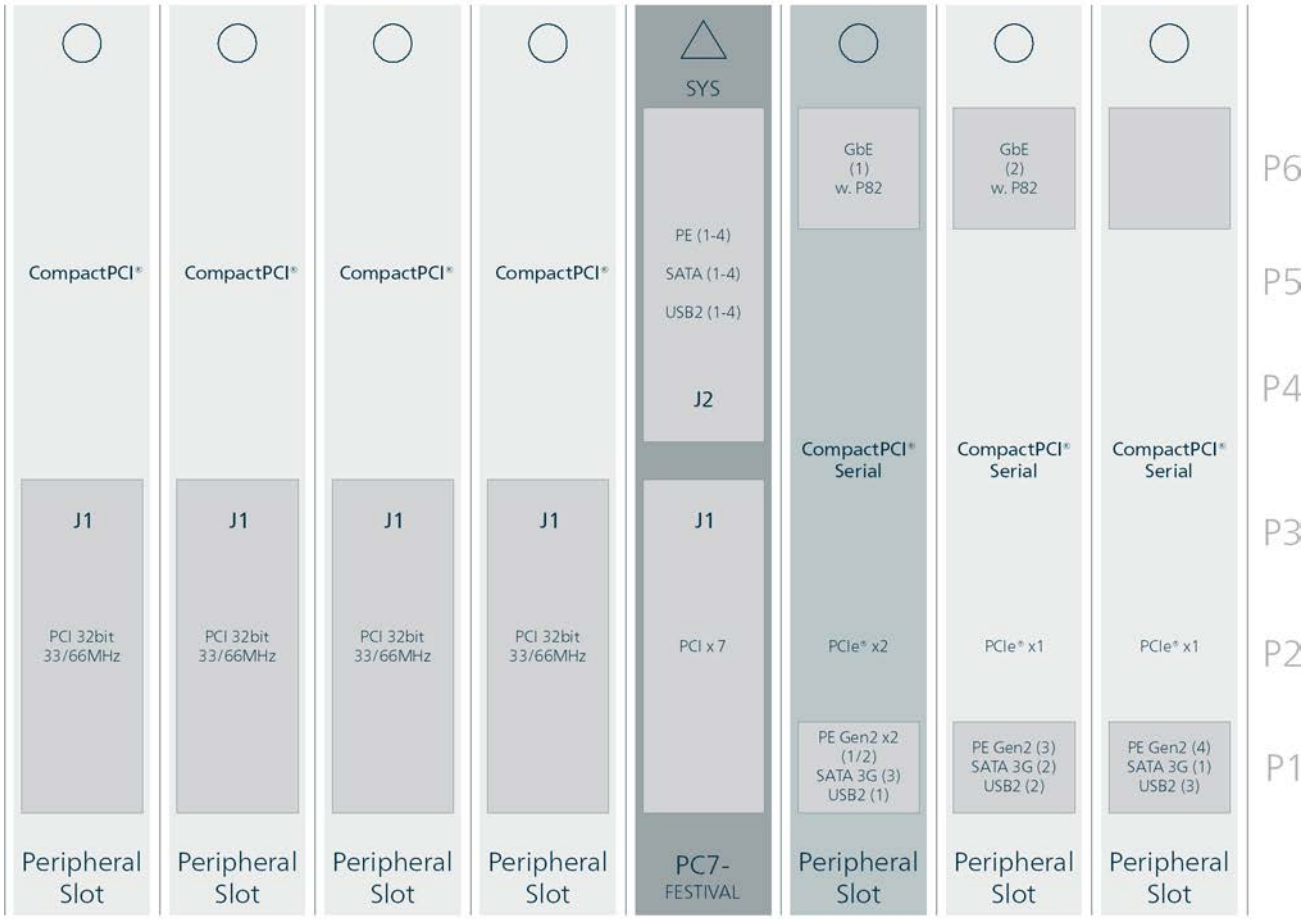
Block Diagram



Backplane Resources



PC7-FESTIVAL • Resources w. 4+1+3 Slots Hybrid Backplane



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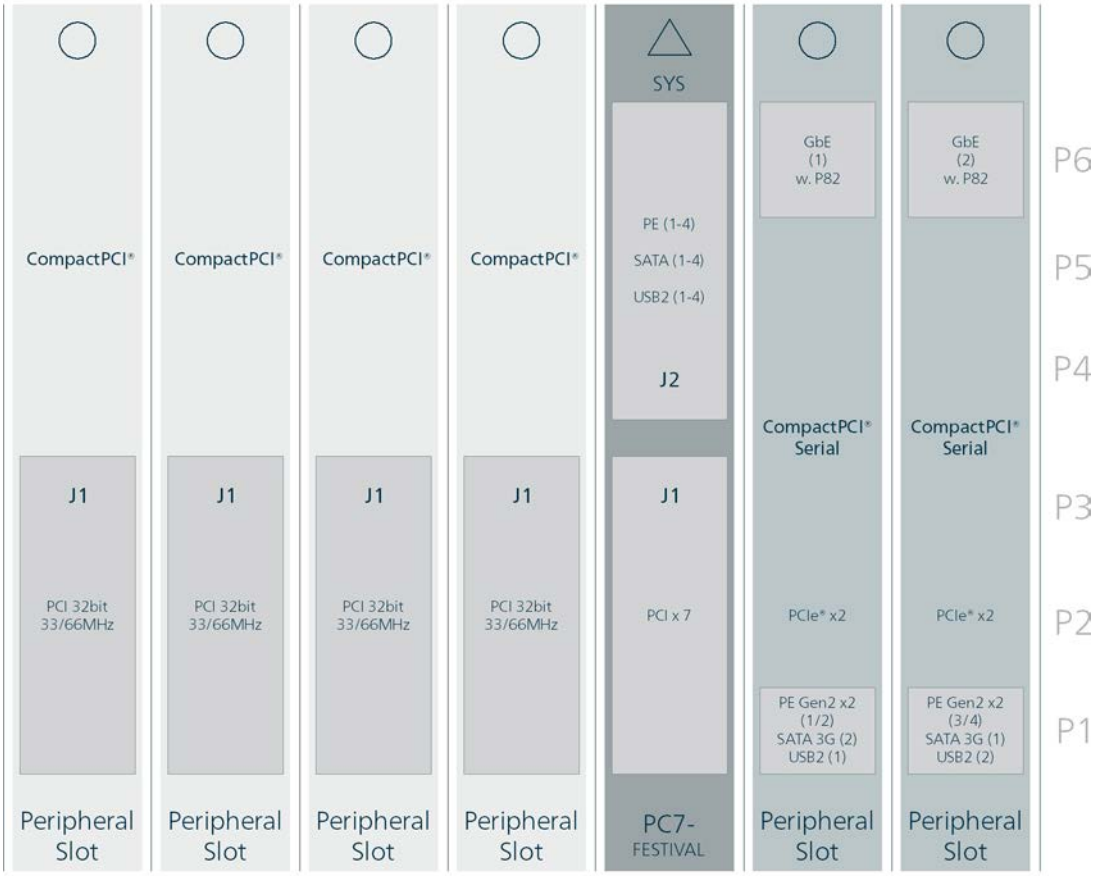
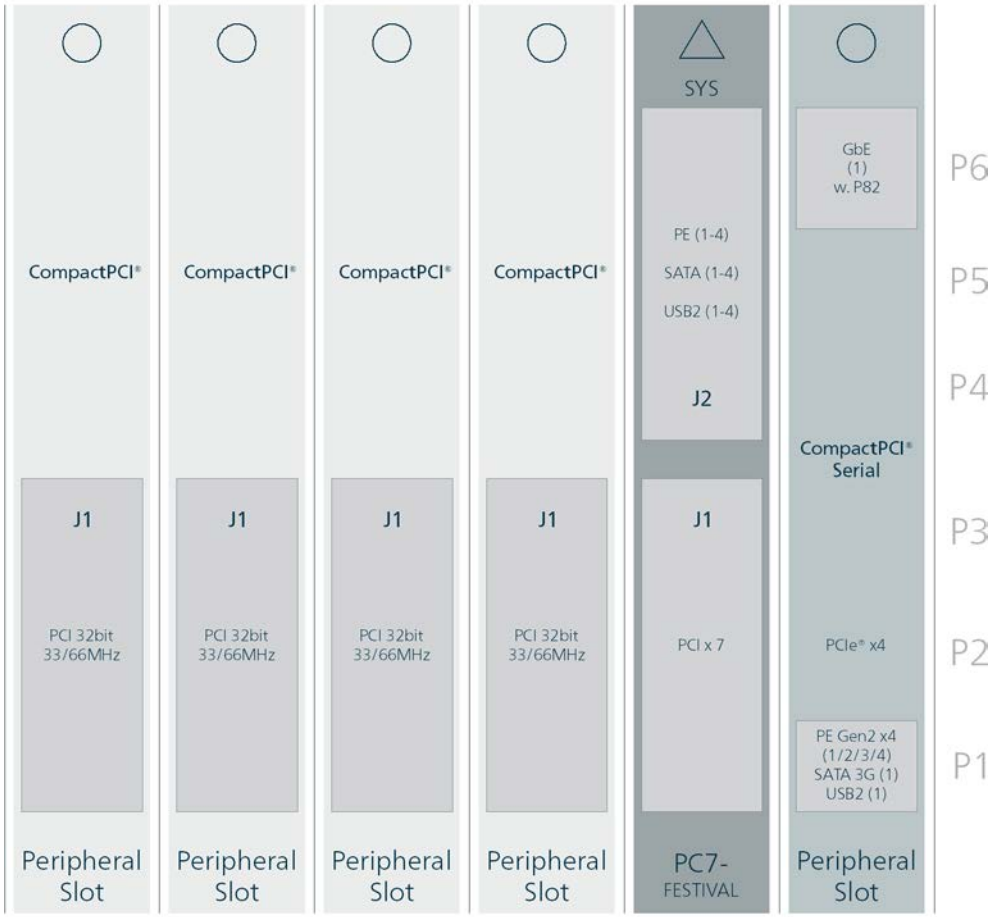
PC7-FESTIVAL • Resources w. 4+1+2 Slots Hybrid Backplane



PC7-FESTIVAL • Resources w. 4+1+1 Slots Hybrid Backplane



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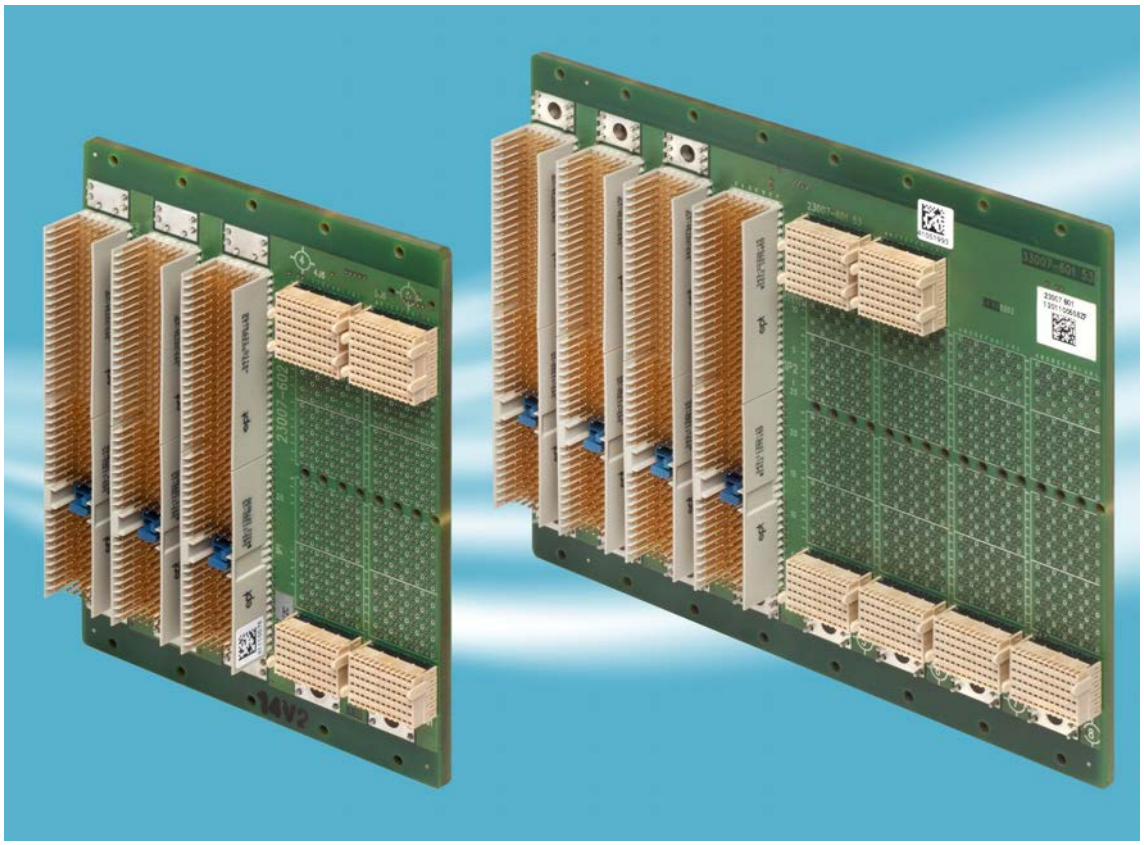
The PC7-FESTIVAL J2 PCIe® lanes must be configured accordingly via BIOS settings to either 4x1, 1x2 + 2x1, 2x2 or 1x4 (4 links, 3 links, two links, single link PCIe®). Connector designations J1/J2 and P1-P6 reflect the CompactPCI® card connector naming convention (mating backplane connectors P1/P2 and J1-J6). A maximum of 4 slots for CompactPCI® Serial peripheral cards can be achieved on a hybrid backplane, and up to 7 slots for CompactPCI® Classic peripheral cards. If the PC7-FESTIVAL CPU card is equipped with a side card (8HP or even 12HP front panel), the adjacent CompactPCI® Serial backplane card slots should be positioned at the same clearance, to prevent loss of usable slots. Such backplanes are highly custom specific - please contact sales@ekf.com.

Backplane Ethernet



Sample Hybrid Backplanes

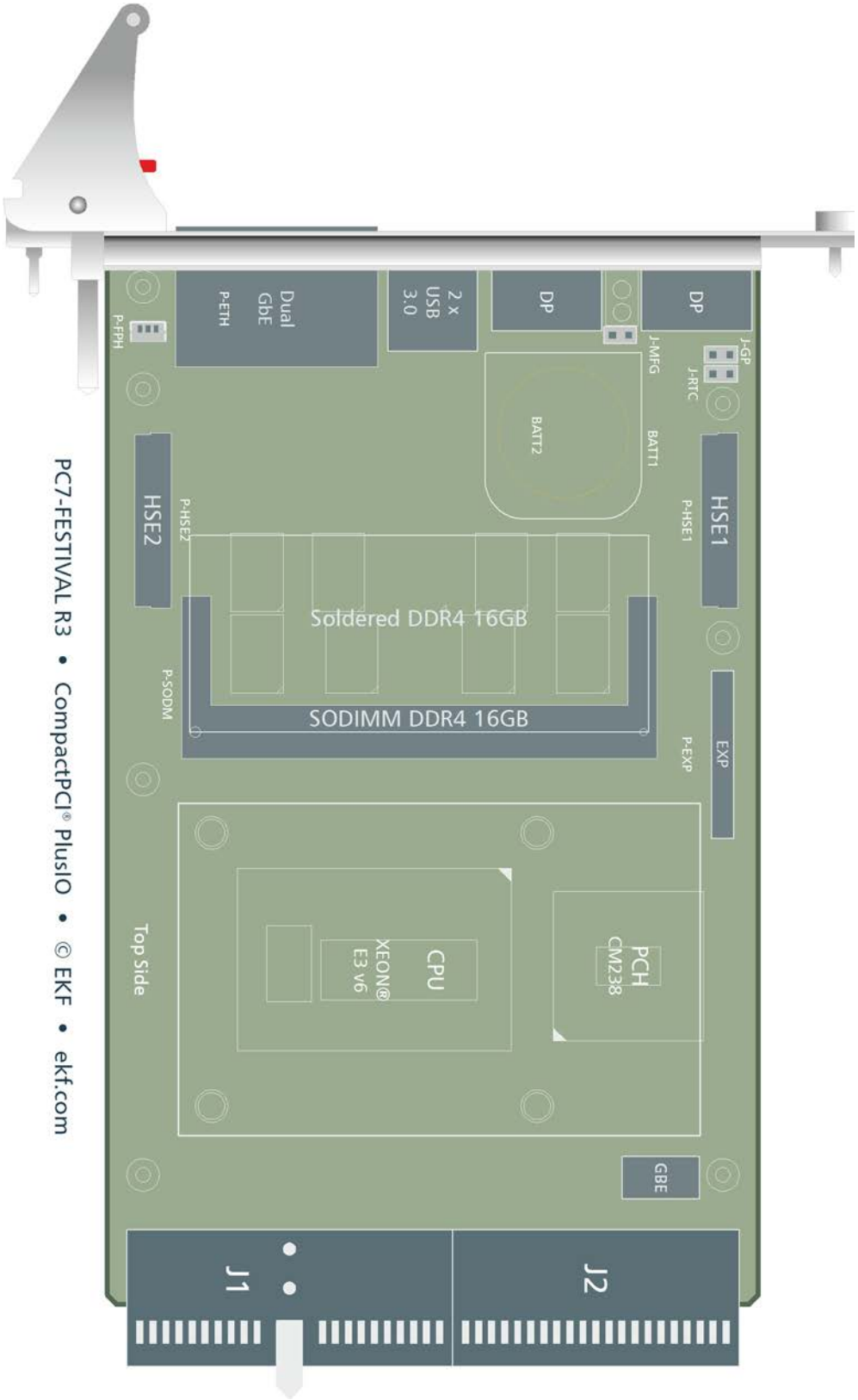
On a hybrid backplane the center slot with P1/P2 connectors is reserved for the CompactPCI® PlusIO CPU card (system slot). To the left there are CompactPCI® classic peripheral card slots (32-bit). On the right side CompactPCI® Serial peripheral cards can be plugged. When backplane Ethernet is required, the low profile mezzanine module P82-GBE can be assembled together with the PC7-FESTIVAL. Then, neighbouring to the CPU card slot, two CompactPCI® Serial slots would be Gigabit Ethernet enabled, via their J6 backplane connectors.

Rear I/O

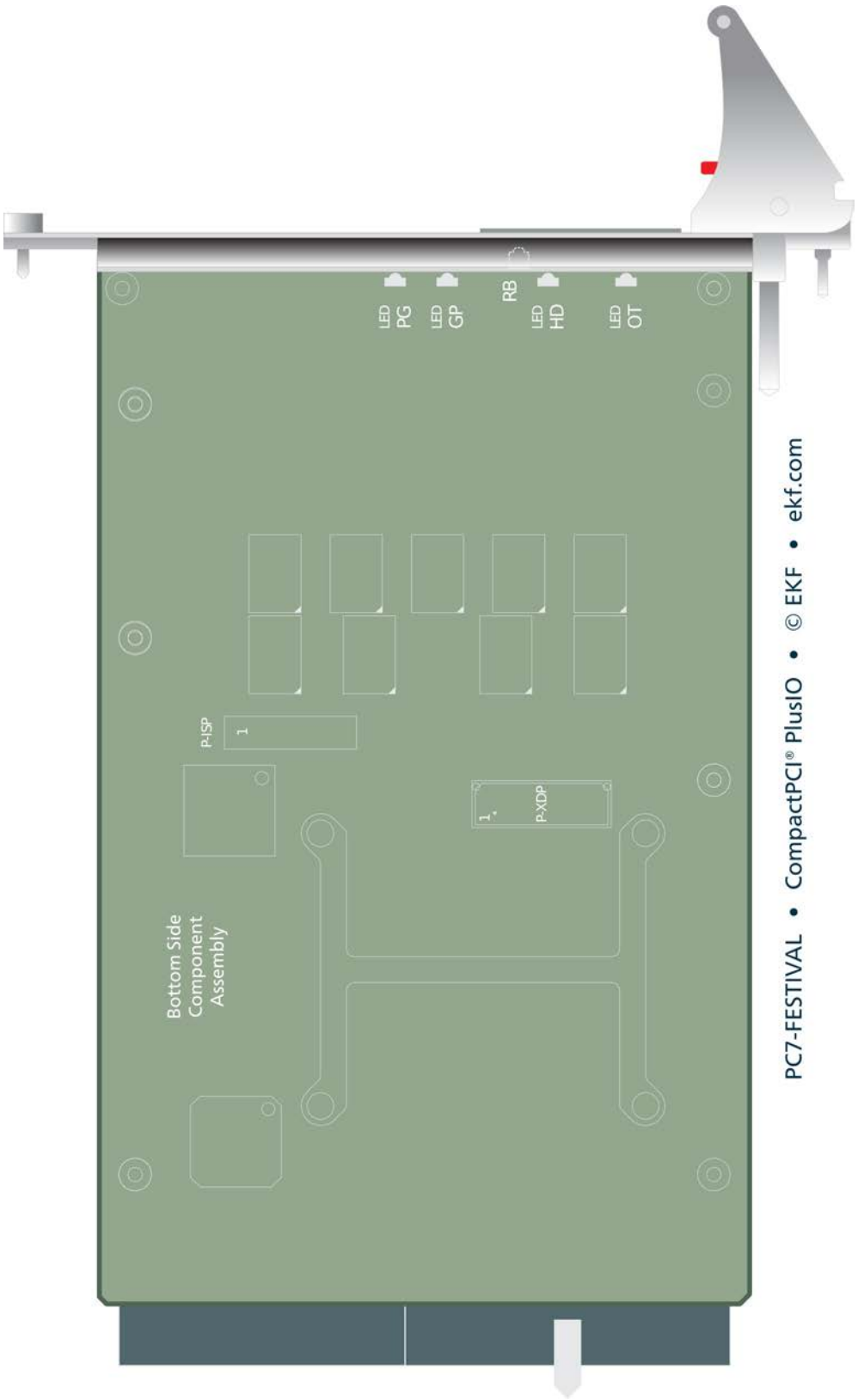
The I/O resources provided by the PC7-FESTIVAL backplane connector J2 can also be used for an rear I/O module. EKF can offer custom specific RIO design - please contact sales@ekf.de.

Sample PlusIO RIO Module

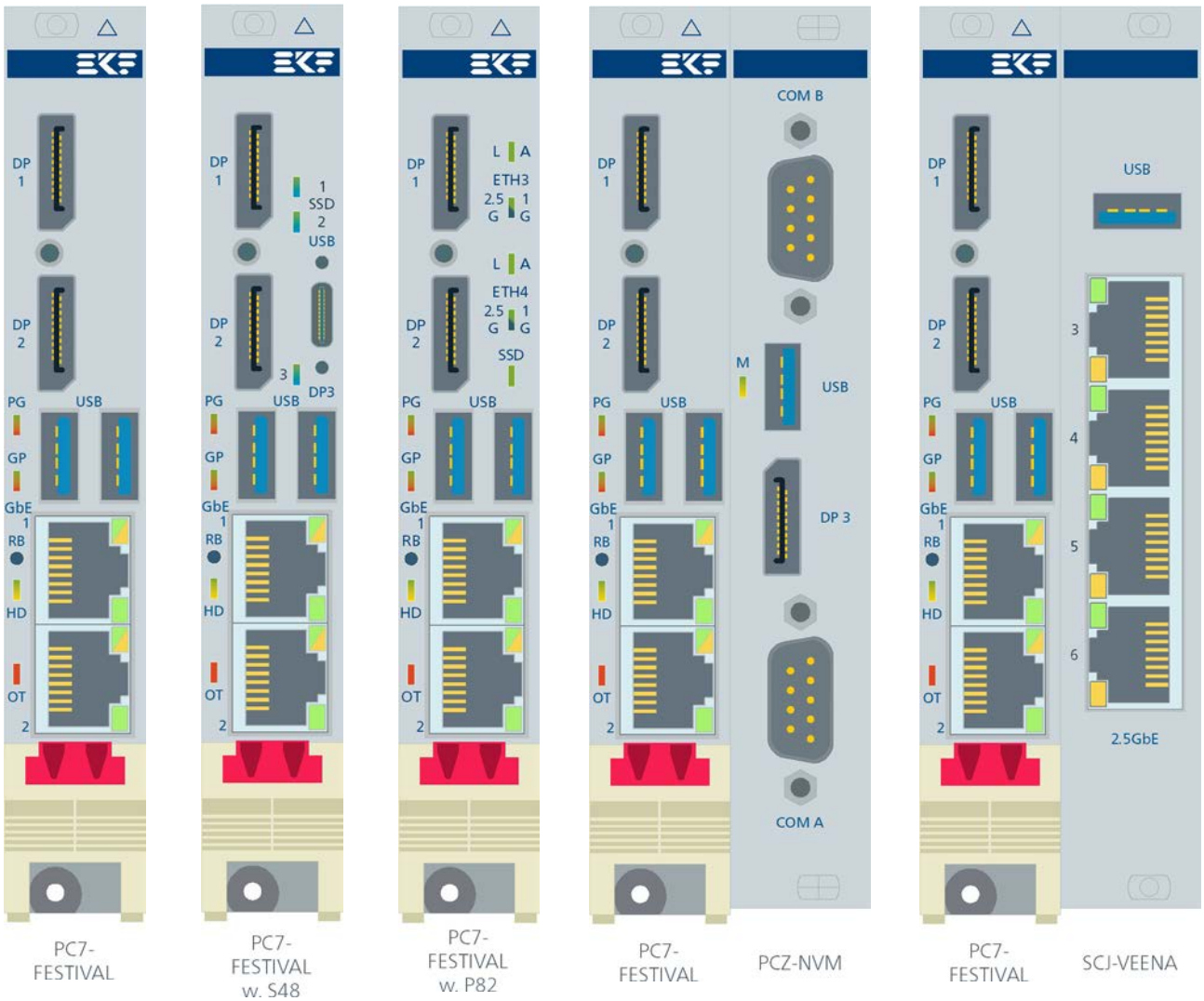
Top View Component Assembly



Bottom View Component Assembly



Front Panel Connectors



ETH 1/2	Dual Gigabit Ethernet RJ-45 receptacles with integrated indicator LEDs
DP 1/2	DisplayPort digital video output receptacles
USB 1/2	Universal Serial Bus 3.0 type A receptacles (USB 3.1 Gen1 SuperSpeed 5Gbps)

Front Panel Switches & Indicators

FPH	Front Panel Handle with integrated switch (programmable function, power event button by default)
GP	General Purpose bicolour LED
HD	Bicoloured LED indicating any activity on SATA ports
OT	LED indicating CPU over-temperature
PG	Power Good/Board Healthy bicolour LED
RB	System Reset Button (Option)

On-Board Connectors & Sockets

P-EXP	Utility EXPansion Interface Connector (LPC, USB, HD Audio, SMBus), interface to optional side board
P-HSE1	High Speed Expansion Connector 1 (4 x PCIe/SATA, 2 x USB), interface to optional low profile mezzanine module or side board
P-HSE2	High Speed Expansion Connector 2 (4 x PCIe, DisplayPort), interface to optional low profile mezzanine module or side board
J1	CompactPCI® Bus 32-bit (universal V(I/O)), 33/66MHz, supports up to 7 peripheral card slots
J2	CompactPCI® PlusIO for rear I/O usage or CompactPCI® Serial peripheral card slots, support for 4 x PCI Express® Gen2, 4 x USB 2.0, 4 x SATA 3Gbps (option)
P-SODM	260-pin DDR4 ECC Memory Module (ECC SODIMM)
P-XDP	CPU Debug Port [1)]

1) Connector populated on customers request only

Pin Headers

P-FPH	Pin header suitable for Front Panel Handle switch cable harness
P-ISP	PLD glue logic device programming connector, not populated

Jumpers

J-GP	Jumper to reset UEFI/BIOS Setup to EKF Factory Defaults, IEEE 1588 Pulse per Second Output
J-MFG	Jumper to enter Manufacturing Mode, not populated
J-RTC	Jumper to reset RTC circuitry (part of PCH), not populated

Microprocessor

The PC7-FESTIVAL is equipped with a member of the 7th generation Intel® processor family: XEON® processor E3 v6 or Core™ processor (code name Kaby Lake H). These dual/quad core low power processors provide integrated graphics and memory controller, which results in a very efficient platform design.

The processors supported by the PC7-FESTIVAL are SKUs with a thermal design power (TDP) of 25-45W. Due to the cTDP feature (configurable TDP) the power consumption of the 45W parts may be lowered by UEFI setup to fit the customers requirements (see table below). The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the chip cannot be removed or changed by the user.

The processors are running at core clock base speeds up to 3 GHz. Due to Enhanced Intel® SpeedStep® and Intel® Turbo Boost Technology each core can decrease or increase its nominal operating frequency in a range from 800 MHz up to 4 GHz. The clock speed is chosen depending on several parameters like the power states of the processor cores/graphics engine, the currently required performance, the actual core temperature etc.

Power is applied across the *CompactPCI*® J1 backplane connector (+12V*, +5V, +3.3V*). The processors core voltage are generated by a switched voltage regulator according to Intels IMVP-8 voltage regulator specification.

* +12V not required on-board, +3.3V not required with 25W TDP processors

Intel® XEON®/Core™ Processors Supported [1)]

Processor Number	Physical/ Logical Cores	Core Clock nom/max [GHz]	Cache [MB]	Gfx Clock [MHz]	Junction Temp. [°C]	TDP [W]	CPU ID	Stepping	SPEC Code
E3-1505L v6	4/8	2.2/3	8	1000	100	25	0x906E9	B-0	SR34X
E3-1505M v6 [2)]	4/8	3/4	8	1100	100	45/35	0x906E9	B-0	SR32K
E3-1501L v6	4/4	2.1/2.9	6	1000	100	25	0x906E9	B-0	
E3-1501M v6 [2)]	4/4	2.9/3.6	6	1000	100	45/35	0x906E9	B-0	
i3-7100E	2/4	2.9/-	3	950	100	35	0x906E9	B-0	SR34V
i3-7102E	2/4	2.1/-	3	950	100	25	0x906E9	B-0	SR34W

1) The processors listed are units with long life support.
2) This processor may run with different TDPs configurable by UEFI settings.

Thermal Considerations

In order to avoid malfunctioning of the PC7-FESTIVAL, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. The processor contains digital thermal sensors (DTS) that are readable via special CPU registers or via PECI bus. DTS allows to get the temperatures of each CPU core separately.

Two further temperature sensors, one of it located in the system hardware monitor NCT7491, allows for acquisition of the boards surface temperature and the thermal state of the onboard system memory channel. Beside this the NCT7491 also keeps a PECI 3.0 master for CPU DTS monitoring and supervises most of the supply voltages. A suitable software on Microsoft Windows® systems to display both, the temperatures as well as the supply voltages, is Speedfan, which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows® taskbar.

The PC7-FESTIVAL is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a *CompactPCI*® board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>20m^3/h or 2m/s (400LFM) around the CPU slot). Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 3m/s (600LFM) or more.

The table showing the supported processors above give also the maximum power consumption (TDP) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows® or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in multiple steps down to 800MHz. Additional a reduction of the graphics core clock (down to 350MHz) and voltage is possible. This leads to an obvious reduction of power consumption resulting in less heating.

A further way to reduce power consumption is achieved by Intels voltage regulators belonging to the IMVP8 standard. These regulators allows the processor to regulate the voltages to the cores, graphics, system agent and other units separately depending on their performance needs. Parts that are currently idle may switched off to save power.

Main Memory

The PC7-FESTIVAL features two channels of DDR4 SDRAMs with support of ECC (Error Correction Code). One channel is realized with 18 memory devices soldered to the board (Memory Down) and delivers a capacity of up to 16GB with a clock frequency of 2400MHz (PC4-2400).

The 2nd channel provides a socket for installing a 260-pin ECC SODIMM module thus allowing a simple expansion of system memory (max. module height = 1.25 inch). Supported are unbuffered DDR4 ECC SODIMMs (72-bit) with V_{DD}=1.2V featuring on-die termination (ODT), according the PC4-2400 specification. Minimum module size is 4GB; maximum module size is 16GB.

Note: DDR4 will not work without the ECC feature on PC7-FESTIVAL.

It is recommended to add a SODIMM module with same size as the Memory Down to get best performance. Since some of the system memory is dedicated to the graphics controller a typically development of 2x8GB of memory is recommended to run operating systems like Windows® 10 or Linux.

The memory controller supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. When in this mode, the memory controller accesses the memory channels in an interleaved way. Since the processors support Intels Flex Memory Technology, interleaved operation isn't limited to systems using memory channels of equal capacity. In the case of unequal memory population the smaller memory channel dictates the address space of the interleaved accessible memory region. The remainder of the memory is then accessed in non-interleaved mode.

In asymmetric mode the memory always will be accessed in a non-interleaved manner with the drawback of less bandwidth. The only meaningful application of asymmetric mode is the special case when only one memory channel is populated (i.e. the SODIMM socket may be left empty).

The contents of the SPD EEPROM on the SODIMM is used by the UEFI/BIOS at POST (Power-on Self Test) to get any necessary timing parameters to program the memory controller within the chipset.

Graphics Subsystem

The graphics subsystems main interfaces like DisplayPort and DVI are part of the processor. Only a few sideband signals (DDC channel, hot plug detection) are located within the PCH CM238.

The PC7-FESTIVAL offers two DisplayPort interfaces with latching receptacle in the front panel. The latching feature prevents DisplayPort cables from detaching in vibrating or harsh environments.

When alternate display interfaces like DVI-I or VGA are required, a variety of converters are available in active or passive form, as adapters or cables.

Independent from the video standard actually in use, DisplayPort, DVI-I or VGA, the VESA DDC standard is supported. This allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. DDC power, +3.3V on DisplayPort connectors, is delivered via electronic switches to protect the board from an external short-circuit condition (1.5A) and to prevent back current flows.

Due to the popular Intel CPU are graphics drivers incorporated within any common operating system.

LAN Subsystem

The Ethernet LAN subsystem is composed of two Gigabit Ethernet ports: One Intel i219LM Physical Layer Transceiver (PHY) using the PCH CM238 internal MAC and one Intel i210IT Gigabit Ethernet Controller. These devices provide also legacy 10Base-T and 100Base-TX connectivity. These Ethernet ports are fed to two RJ45 jacks located in the front panel. Each port includes the following features:

- One PCI Express lane per Ethernet port (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability.
- Half- or full-duplex operation.
- IEEE 802.3u, 802.3ab Auto-Negotiation for the fastest available connection.
- Jumperless configuration (complete software-configurable).

Two bicoloured LEDs integrated into the dedicated RJ-45 connector in the front panel are used to signal the LAN link, the LAN connection speed and activity status.

Each device is connected by a single PCI Express lane to the PCH. Their MAC addresses (unique hardware number) are stored in dedicated FLASH/EEPROM components. The Intel Ethernet software and drivers for the i219LM and i210IT are available from Intel's World Wide Web site for download.

When managing the board by Intel Active Management Technology (iAMT), the dedicated network port to do so is accessible by the RJ45 connector GbE1 (the upper port within the front panel).

The i210 controller supports the IEEE 1588 Precision Time Protocol (the one connected to the lower port within the front panel (GbE2)) and is capable to generate Pulse per Second (PPS) and Pulse per Minute (PPM) signals that may be routed to the jumper J-GP and the *CompactPCI®* PlusIO connector J2. These signals can be used to trigger events on Mezzanine Side Boards or Peripheral Boards. The following routing is possible by UEFI/BIOS settings:

- Pulse per Second (PPS): J-GP Pin 1 and CompactPCI® SATA SCL J2 Pin D14
- Pulse per Minute (PPM): CompactPCI® SATA SDO J2 Pin D13

As an option, two 4-speed 2.5GBASE-T ports are available from the backplane, by means of the P82-GBE low profile mezzanine module (from PCB Rev. 2022 off).

Serial ATA Interface (SATA)

The PC7-FESTIVAL provides a total of up to ten serial ATA (SATA) ports, derived from up to three independent SATA controllers. All of these ports support data transfer rates of 6Gbps (600MB/s), 3Gbps (300MB/s) or 1.5Gbps (150MB/s). SATA controllers are located within the CM238 Platform Controller Hub that holds up to 6 SATA interfaces (depends on the configuration on expansion interface P-HSE1).

Up to four of the CM238 ports are fed to the high speed expansion connector P-HSE1. This connector allows the installation of low profile expansion boards like C41-CFAST or C42-SATA to attach the popular CFast cards or Micro SATA SSDs (1.8-inch) respectively. Another mezzanines are the C47-MSATA and C48-M2, carriers for two MSATA or M.2 SSD modules, respectively.

A LED named HD located in the front panel, signals disk activity status of any CM238 SATA devices (green).

Additionally a variety of side cards is available, suitable for mounting on the PC7-FESTIVAL in a 4HP (20.32mm) distance (resulting in 8HP front panel width for the assembly). Some of these side boards can accommodate a SATA drive, e.g. a 2.5-inch SSD.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® and Linux.

PCI Express® Interface

The PC7-FESTIVAL is provided with several PCI Express (PCIe) lanes for I/O expansion. The CM238 offers a total of up to sixteen PCI Express ports supporting PCIe Gen 3 speed (8GT/s).

Three of them are used to operate the two Ethernet Controllers (i219LM and i210IT) and the PCIe to PCI Bridge (PI7C9X112). Four ports are connected to the CompactPCI® connectors J2 (four lanes), four to the high speed expansion connector P-HSE2.

Four combo ports are fed to the local expansion interface connector P-HSE1, that may work as PCIe (1x4 or 2x2) or as SATA ports, strapped dynamically by configuration signals on P-HSE1.

Possible settings are

- One PCIe link x 4
- Two PCIe links x 2
- Four SATA links
- One PCIe link x 2, two SATA links

By default the PCIe lanes connected to the 2nd high speed expansion connector P-HSE2 build four PCIe links with one lane. Alternative configurations (1x4 or 2x2) are possible by programming soft-straps within the PC7 firmware image. Ask EKF if changes are required.

See sections “P-HSE1" and “P-HSE2" from “Mezzanine Connectors" for further details.

Universal Serial Bus (USB)

The PC7-FESTIVAL is provided with fourteen USB ports. All of them are USB 2.0 capable, but six ports are also supporting the USB 3.0 SuperSpeed standard. Two USB 3.0 interfaces are routed to front panel connectors and one is connected to P-HSE1 interface.

The USB 2.0 interfaces are distributed to the front panel (two ports), two to the high speed expansion connector P-HSE1, and four ports are available across the backplane connectors for CompactPCI® J2.

The front panel USB connectors can source a minimum of 1.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interface P-HSE1 and on the CompactPCI® connectors is located on expansion boards and the boards on the CompactPCI® backplane respective. The USB xHCI controllers handling the USB port operation at SuperSpeed, high-speed, full-speed and low-speed are integrated into the CM238 PCH.

Utility Interfaces

Besides the high speed mezzanine interface connectors P-HSE1 and P-HSE2, the PC7-FESTIVAL is provided with the utility interface expansion connector socket P-EXP. This connector comprises several interfaces, which may be useful for system expansion on mezzanine cards, as an option:

- HD Audio
- LPC (Low Pin Count)
- I^2C
- 2 x UART (TTL)

The I^2C is connected to controller $I^2C[0]$ of the CM238 platform controller hub. The I^2C signal lines on the P-EXP utility expansion connector are also routed to P-HSE2.

The HD Audio port requires an additional audio codec, as provided e.g. on the SCS-TRUMPET side card.

The LPC bus presents an easy way to add legacy interfaces to the system. EKF offers a variety of mezzanine expansion boards (side cards), to be attached on top of the PC7-FESTIVAL, featuring all classic Super-I/O functionality, for example the SCS-TRUMPET or PCS-BALLET. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel.

Real-Time Clock

The PC7-FESTIVAL has a time-of-day clock and 100-year calendar, integrated into the CM238 PCH. A battery on the board keeps the clock current when the computer is turned off. The PC7-FESTIVAL uses a holder to keep a CR2032 lithium coin cell, giving an autonomy of more than 5 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Alternately a CR2032 battery can be soldered in the board when board coating or shock/vibration is an interest.

In applications were the use of a battery is not permitted, a SuperCap can be soldered instead of the battery.

It is also possible to use the PC7-FESTIVAL without any battery or SuperCap. In this case the Real-Time Clock can't keep its time and date. Per default an error message is reported by the UEFI/BIOS during boot in all cases, where the Real-Time clock settings are bad:

```
00C08270: Real Time Clock Error - Check Date and Time settings
```

```
00C08251: System CMOS Checksum bad
```

To suppress this message a setup node exists within the UEFI/BIOS (Build #132 or later):

- After Power-On press function key <F2> to enter setup menu
- Advanced → Advanced Menu → ME Configuration → ME Unconfig on RTC Clear → Disabled

SPI Flash

The UEFI/BIOS and iAMT firmware is stored in flash devices with Serial Peripheral Interface (SPI). Up to 16MByte of UEFI code, firmware and user data may be stored nonvolatile in these SPI Flashes.

The SPI Flash contents can be updated by an UEFI Shell, DOS or Linux based tool. This program and the latest PC7-FESTIVAL UEFI/BIOS binary are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the PC7-FESTIVAL may no more be operable. In this case you would possibly have to send in the board, because the Flash device is directly soldered to the PCB and cannot be changed by the user.

Reset

The PC7-FESTIVAL is provided with several supervisor circuits to monitor supply rails like the CPU core voltage, 1.2V, 3.3V or 5V.

To force a manual board reset, the PC7-FESTIVAL offers a small tactile switch within the front panel. This push-button is indent mounted and requires a tool, e.g. a pen to be pressed, preventing from being inadvertently activated.

The handle within the front panel contains a micro switch that is used to generate a power button event. By pressing the handle's red push button a pulse is triggered.
Animated GIF: www.ekf.com/c/ccpu/img/reset_400.gif

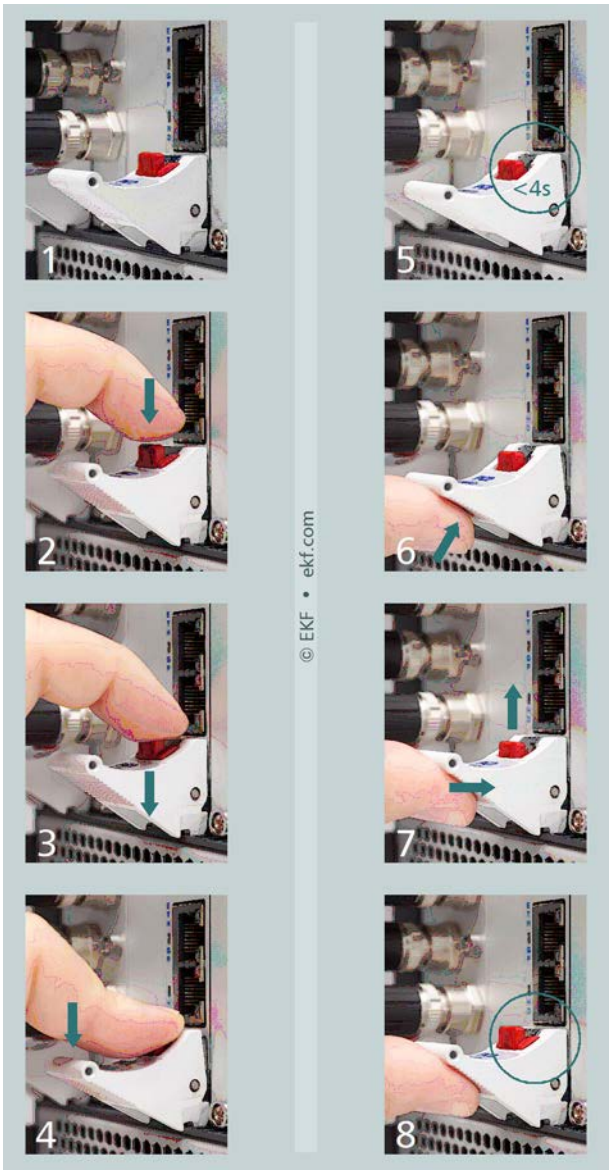
Note: To prevent the board to cause a power button override, the handle should be closed immediately after unlocking the front panel handle. A power button override is triggered by opening the front panel handle for at least 4 seconds, which results in bringing the board to power state S5. In case of entering this state, unlock and lock the front panel handle a 2nd time to reenter normal power state S0 again. See also section 'PG (Power Good) LED' to see how the PC7-FESTIVAL indicates the different power states.

Warning: The PC7-FESTIVAL will enter the power state S5 if the front panel handle is not closed properly when the system powers up. An open handle is signalled by a yellow blinking ‘PG LED’.

The manual reset push-button and the power button functionality of the front panel handle could be passivated by UEFI/BIOS settings.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI® PlusIO connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the tactile reset switch.

The healthy state of the PC7-FESTIVAL is indicated by the LED PG (Power Good) located in the front panel. This bicoloured LED signals different states of the board (see section below). As soon as this LED begins to lite green, all power voltages are within their specifications and the reset signal has been deasserted.



https://www.ekf.com/c/ccpu/img/reset_400.gif

Watchdog

An important reliability feature is a software programmable watchdog function. The PC7-FESTIVAL contains two of these watchdogs. One is part of the CM238 PCH and also known as TCO Watchdog. A detailed description is given in the CM238 data sheet. Operating systems like Linux offer a driver interface to the TCO watchdog.

The behaviour of the 2nd watchdog is defined within a PLD of the PC7-FESTIVAL, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After programming the time-out value and arming the WD, the related software (e.g. application program) must trigger the watchdog periodically. For details on programming the watchdog see section “Board Control and Status Register (BCSR)”.

This watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a full system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it has been put on alert, whereas it is possible to reprogram its time-out value at any time.

Front Panel LEDs

The PC7-FESTIVAL is equipped with four LEDs which can be observed from the front panel. Three of these LEDs are labelled according to their primary meaning, but should be interpreted altogether for system diagnosis:

LED			Status
PG Green/Red	GP Green/Red	HD Green/Yellow	
OFF	GREEN	GREEN	Sleep State S5 (Soft Off)
OFF	GREEN	OFF	Sleep State S4 (Suspend to Disk/Hibernate)
OFF	OFF	GREEN	Sleep State S3 (Suspend to RAM/Standby)
GREEN	RED BLINK	X	After Reset
GREEN	X	X	Board Healthy and in S0 State
YELLOW BLINK	X	X	Front panel handle is unlocked
RED	X	X	Hardware Failure - Power Fault
RED BLINK	X	X	Software failure (reserved)

PG (Power Good) LED

The PC7-FESTIVAL offers a bicolour LED labelled PG located within the front panel. After system reset, this LED defaults to signal different power states:

- Off Sleep state S3, S4 or S5
- Green Healthy
- Yellow blink Front panel handle open
- Red steady Hardware failure
- Red blink Software failure (reserved for future use)

To enter the PG LED state *Software Failure,* the bit PGLED in the board control register CTRLL_REG must be set. The PG LED remains in this red blinking state until this bit is cleared. After that it falls back to its default function.

GP (General Purpose) LED

This programmable bicolour LED can be observed from the PC7-FESTIVAL front panel. The status of the red part within the LED is controlled by the GPP_D11 of the PCH CM238. Setting GPP_D11 to “1" will switch on the red LED. Turning on or off the green LED is done by setting the bit GPLED in the board control register CTRLH_REG.

The GP LED is not dedicated to any particular hardware or firmware function with exception of special power states of the LED PG as described above. Nevertheless, a red blinking GP LED is an indication that the UEFI/BIOS code couldn't start.

While the CPU card is controlled by the UEFI/BIOS firmware, the GP LED is used to signal board status information during POST (Power On Self Test). After successful operating system boot, the GP LED may be freely used by customer software. For details please refer to http://www.ekf.de/p/pc7/firmware/relnotes.txt.

HD (Hard Disk Activity) LED

The PC7-FESTIVAL offers a bicoloured LED marked as HD placed within the front panel. This LED, when blinking green, signals activity on any device attached to the SATA ports of the CM238.

As previously described, the green part of this LED may change its function dependent on the state of the LED PG.

OT (Processor Hot) LED

The thermal status of the processor can be monitored exactly by several utilities that are available in the market (e.g. “Speedfan” for Windows® or “lmsensors” for Linux). The LED “OT” (over-temperature) can be assumed as a summery of that. It shows when the processor impends to get too hot, resulting in reducing its performance by Intel® Speed Step® or similar.

Power Supply Status (PWR_FAIL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions to the CompactPCI® specification and may bedriven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possiblefailure. On the PC7-FESTIVAL DEG# is pulled to VCC and FAL# is routed to GPP_D0 of the CM238 PCH.

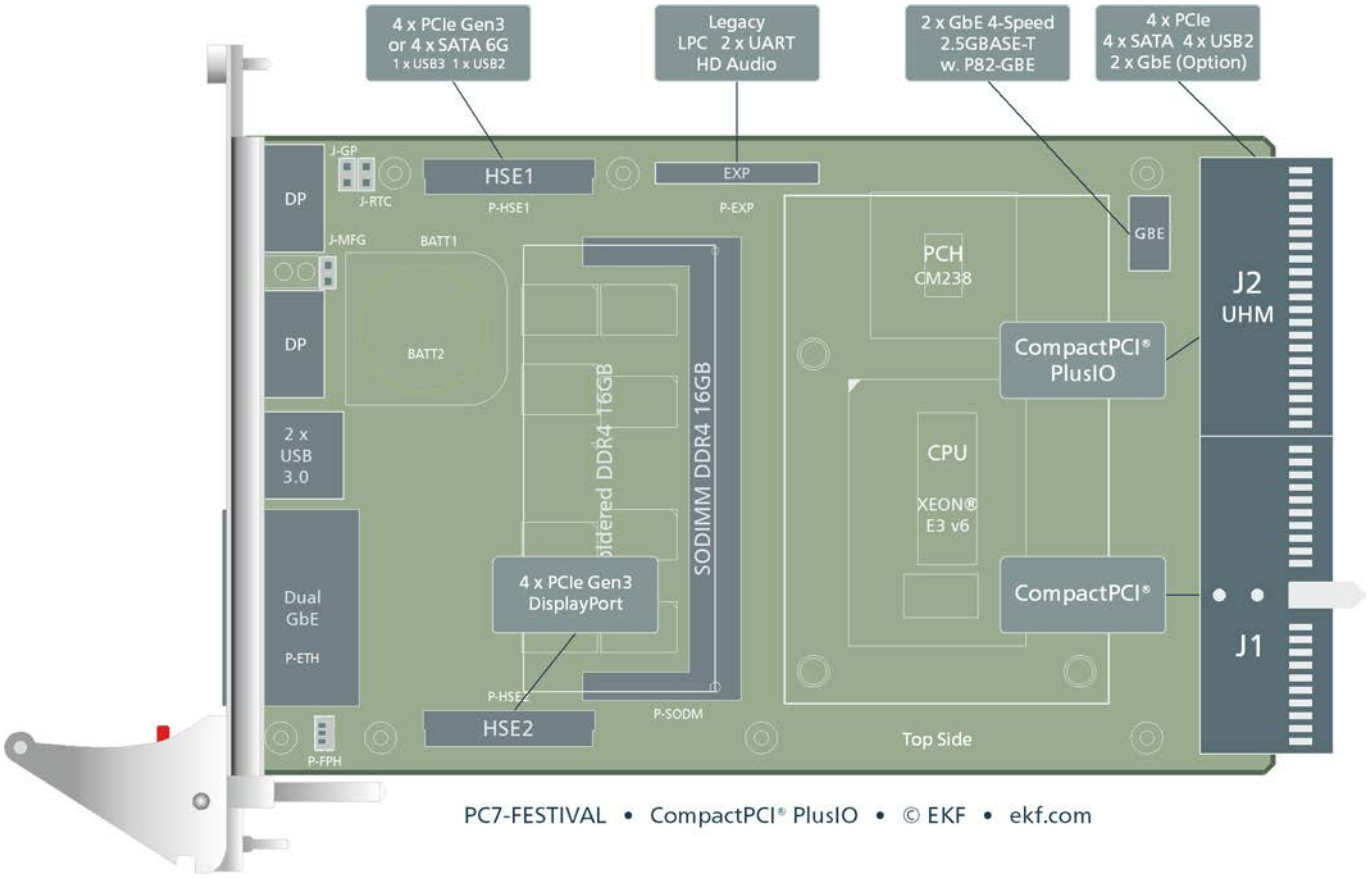
As an option a circuit can be stuffed on PC7-FESTIVAL to use this signal as an output to drive PSON# of a power supply. With this option and the related external wiring it is possible to switch off the mainpower supply when the system powers down to state S4. To restart the system, the PSON# line mustbe pulled down manually for a second approximately, e.g. by an external push-button.

The use of this signal as PWR_FAIL# or PSON# is mutually exclusive.

Mezzanine Side Board Options

The PC7-FESTIVAL is provided with several stacking connectors for attachment of a mezzanine expansion module (aka side board), suitable for a variety of readily available mezzanine cards (for a more comprehensive overview, please refer to www.ekf.com/s/mezzanine_connectors.pdf). EKF furthermore offers custom specific development of side boads (please contact sales@ekf.de).

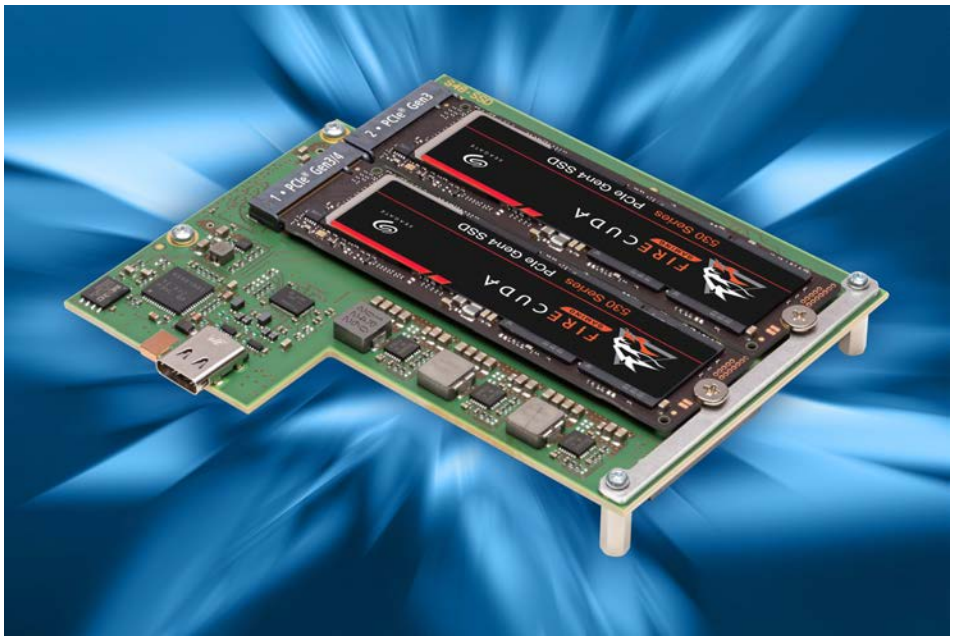
Most mezzanine expansion modules require an assembly height of 8HP in total, together with the CPU carrier board (resulting from two cards at 4HP pitch each). In addition, cropped low profile mass storage mezzanine modules can be attached to P-HSE, which maintain the 4HP envelope, for extremely compact systems.



PC7-FESTIVAL • System Expansion Options

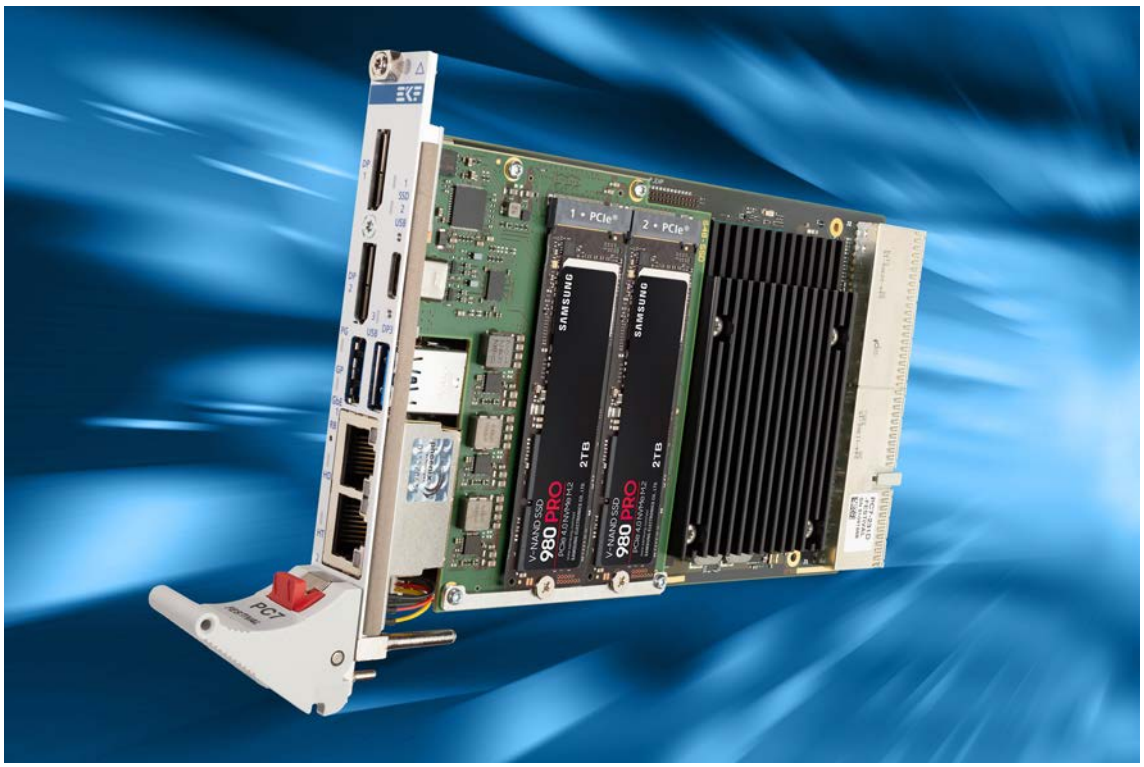
New from PCB Rev. 2022 off: Expansion Connector GBE for passing 2 x 2.5GBASE-T to J2, as an option with P82 low profile mezzanine module.

Low Profile NVMe® Mezzanine Mass Storage 4HP



S48-SSD • Dual M.2 NVMe SSD Low Profile Mezzanine

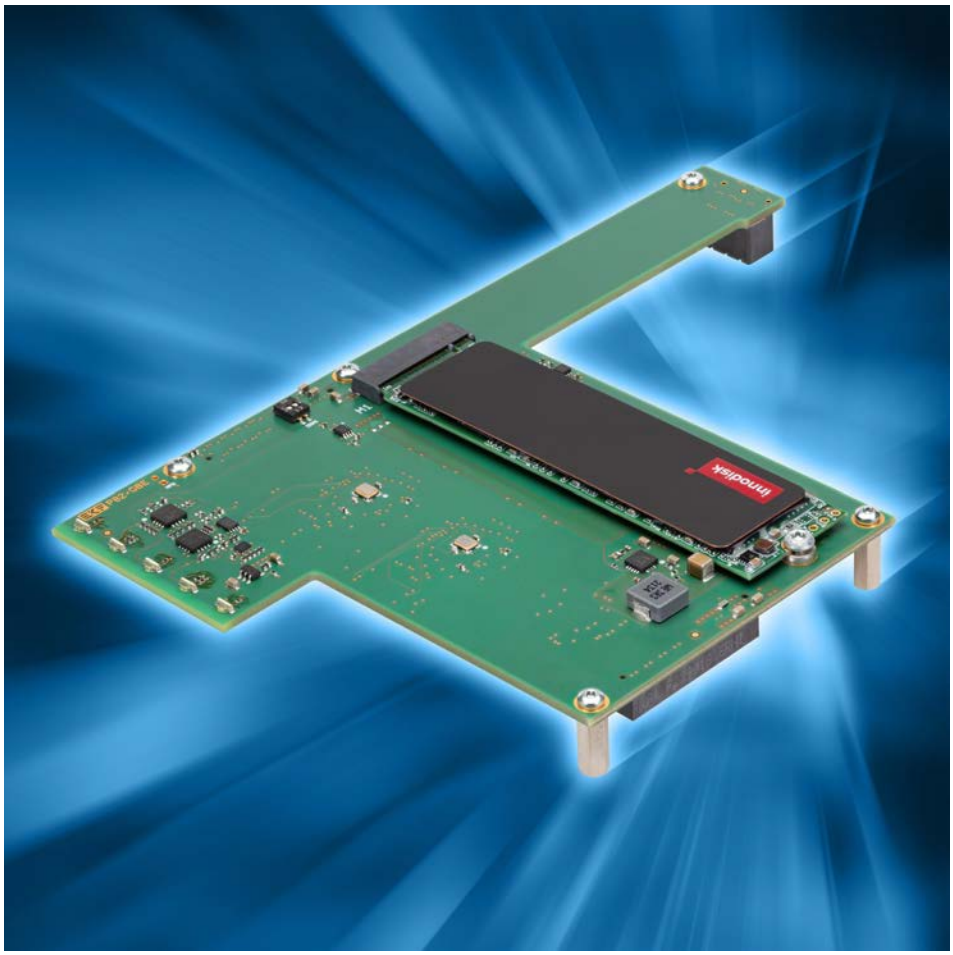
4HP Assembly • PC7-FESTIVAL w. S48-SSD



4HP Assembly w. S48-SSD

Low Profile 4HP NVMe® Storage & Backplane 2.5G Ethernet

4HP Assembly w. P82-GBE



P82-GBE

4HP Assembly w. P82-GBE

4HP Assembly • PC7-FESTIVAL w. P82-GBE

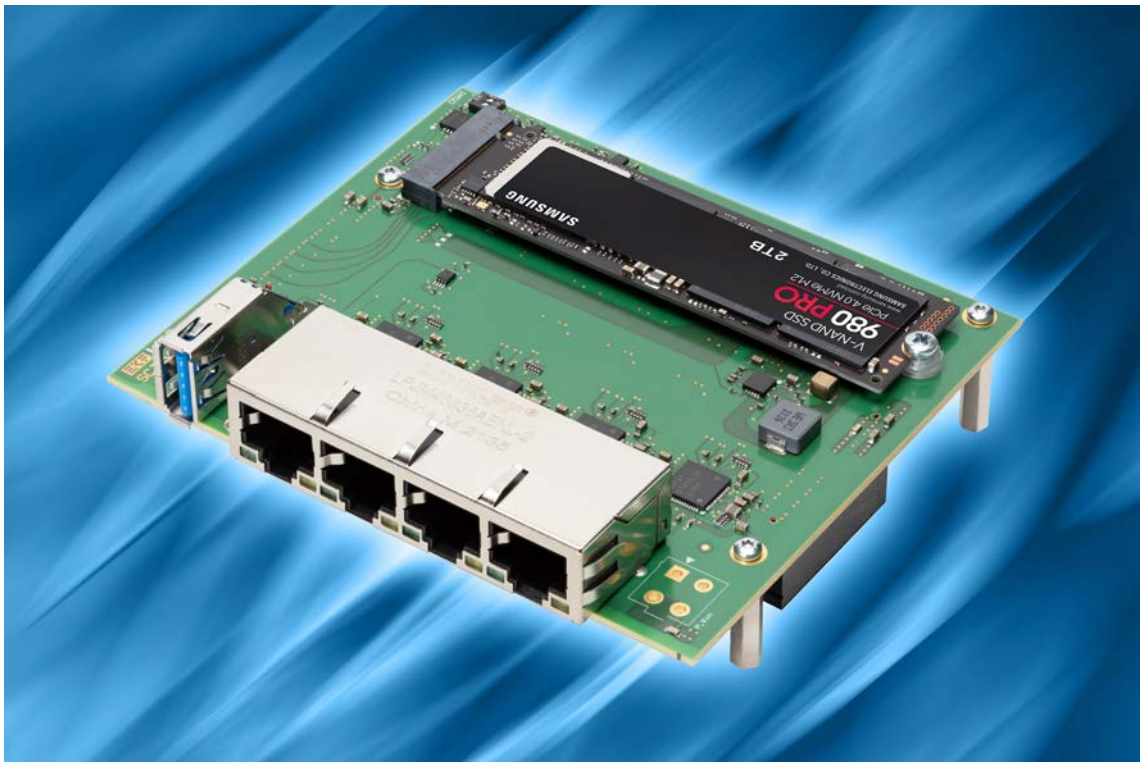
Low Profile SATA Mezzanine Mass Storage 4HP

C48-M2 • Low Profile Mezzanine Dual M.2 SATA SSD

4HP Assembly • PC7-FESTIVAL w. C48-M2

4HP Assembly w. C48-M2

Side Card Assemblies 8/12HP



SCJ-VEENA • Quad 2.5GBASE-T NICs & M.2 NVMe

8HP Assembly • PC7-FESTIVAL w. SCJ-VEENA

8HP Assembly • PC7-FESTIVAL w. SCJ-VEENA

8HP Assembly • PC7-FESTIVAL w. SCJ-VEENA

8HP Assembly • PC7-FESTIVAL w. SCL-RHYTHM

8HP Assembly • PC7-FESTIVAL w. PCU-UPTEMPO (Similar Photo)

8HP Assembly • PC7-FESTIVAL w. PCU-UPTEMPO (Similar Photo)

8HP Assembly w. PCZ-NVM

8HP Assembly w. PCZ-NVM

8HP Assembly w. PCZ-NVM

12HP Assembly w. PCZ-NVM & C32-FIO

Mezzanine Connectors Related Documents
www.ekf.com/s/mezzanine_connectors.pdf

P-EXP	
I/F Type	Controller
LPC (Low Pin Count)	PCH
HD Audio	PCH
I^2C	PCH (I^2C[0])
2 x UART (TTL)	PCH

P-HSE1	
I/F Type	Controller
4 x PCIe Gen3 or 4 x SATA 6Gbps	PCH
2 x USB 2.0, 1 x USB 3.0	PCH

P-HSE2	
I/F Type	Controller
4 x PCIe Gen3	PCH
1 x DisplayPort	PCH
I^2C	PCH (I^2C[0])

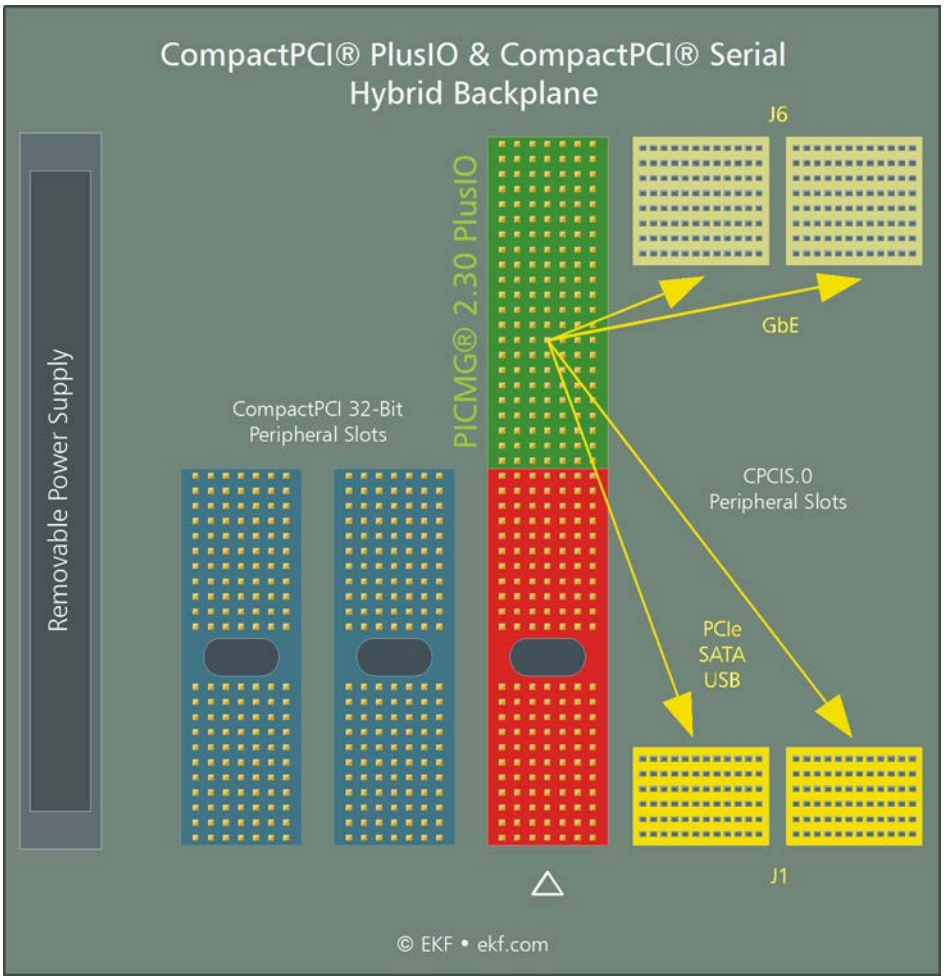
P-GBE (from PCB Rev.3 off)	
I/F Type	Controller
2 x 2.5GBASE-T Ethernet 4-Speed	2 x I226-IT P82-GBE Low Profile Mezzanine

CompactPCI® PlusIO

CompactPCI® PlusIO (PICMG® 2.30) is a standard for rear I/O across J2. High speed signal lines (PCI Express®, SATA, Gigabit Ethernet and USB) are passed from the PC7-FESTIVAL through the special UHM J2 connector to the backplane, for usage either with a PlusIO rear I/O transition module, or CompactPCI® Serial card slots.

CompactPCI® Serial (PICMG® CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. On a hybrid backplane, both card styles can reside, CompactPCI® and CompactPCI® Serial, with the PC7-FESTIVAL in the middle as controller for both backplane segments.

The PC7-FESTIVAL can be used in any system with a CompactPCI® PlusIO backplane according to the PICMG® 2.30 specification. Hybrid backplanes allow the configuration of systems with CompactPCI® Serial slots in addition to classic CompactPCI® boards.



Sample Small Systems Hybrid Backplane

As an alternate to a hybrid backplane, the PC7-FESTIVAL can be combined with a CompactPCI® PlusIO rear I/O transition module.

Warning: Do not operate the standard PC7-FESTIVAL in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignment of a 64-bit CPCI backplane differs substantially from a CompactPCI® PlusIO backplane, which will result in an overvoltage or short circuit situation on several pins, causing permanent damage to the PC7-FESTIVAL . For use together with a 64-bit CompactPCI® classic backplane, special PC7-FESTIVAL versions are available on customer request, however supporting only 32-bit peripheral cards. The use of 64-bit CompactPCI® classic peripheral boards may cause problems.

Board Hot-Plug

Hot-plug of the PC7-FESTIVAL is not supported, no matter whether it is working as a system controller or satellite board. But it is possible for the PC7-FESTIVAL to detect and handle hot-plug events of peripheral boards. This feature is supported on all interfaces fed to the CompactPCI PlusIO backplane, i.e.

- PCI Express
- SATA
- USB
- Gigabit Ethernet

Except of PCI Express, hot-plug is enabled on all interfaces by default. For PCI Express the UEFI/BIOS (Build #138 or later) setup of the PC7-FESTIVAL provides settings to switch on or off the hot-plug feature, for Fat Pipe or Standard peripheral slots on different menu places:

- After Power-On press function key <F2> to enter setup menu
- Fat Pipe Slots:
  Advanced→Advanced Menu→PCI Configuration→SA PCI Express Configuration→Hot-Plug
- Standard Slots:
  Advanced→Advanced Menu→PCI Configuration→PCH PCI Express Configuration
  PCH PCIe Root Port [5-8/19/20]→Hot-Plug

Supplementary Information

Useful Information Related to CompactPCI® Serial	
CompactPCI® Serial Overview	www.ekf.com/s/serial_concise.pdf
CompactPCI® PlusIO Overview	www.ekf.de/p/plusio.pdf

Installing and Replacing Components

Before You Begin

Warning: The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution: Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning: This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI® slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning: This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Identify the board, be sure to touch the board only at the front panel
- Unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning: Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery should last during the lifetime of the PC7-FESTIVAL.

However, some versions of PC7-FESTIVAL are delivered with a battery holder which makes it possible for the user to replace the coin cell. Use a CR2032 cell as replacement part to ensure an extended temperature range. Be careful when removing the old cell and inserting the new one.

For boards with a soldered battery the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning: Danger of explosion if the battery is incorrectly replaced or shorted. Replace only with the same or equivalent type. Do not expose a battery to fire.

Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. Several devices are part of the processor and platform controller hub CM238.

Bus #	Device #	Function #	Vendor ID	Device ID	Description
0	0	0	0x8086	0x5918	Processor Host Bridge/DRAM Controller
0	2	0	0x8086	0x591D	Processor Integrated Graphics Device
0	8	0	0x8086	0x1911	Gaussian Mixture Model Device
0	20	0	0x8086	0xA12F	USB 3.0 xHCI Controller
0	20	2	0x8086	0xA131	Thermal Subsystem
0	21	0-1	0x8086	0xA160-A161	I^2C Controller #0-1
0	22	0-1	0x8086	0xA13A-A13B	Intel ME Interface #1-2
0	22	2	0x8086	0xA13C	Intel ME IDE Redirection
0	22	3	0x8086	0xA13D	Intel ME Keyboard Text Redirection
0	22	4	0x8086	0xA13E	Intel ME Interface #3
0	23	0	0x8086	0xA102 0xA106	SATA: AHCI Mode [1] SATA: RAID Capable [2]
0	27	0-1	0x8086	0xA169-A16A	PCH PCI Express Root Port #19-20 (→ CPCI-S.0)
0	28	2	0x8086	0xA112	PCH PCI Express Port #3 (→ Intel i210IT)
0	28	4-7	0x8086	0xA114-A117	PCH PCI Express Port #5-8
0	29	0-3	0x8086	0xA118-A11B	PCH PCI Express Port #9-12 (→ HSE2)
0	29	4	0x8086	0xA11C	PCH PCI Express Port #13 (→ x4 HSE1)
0	30	0-1	0x8086	0xA127-A128	UART Controller #0-1
0	31	0	0x8086	0xA154	LPC Bridge
0	31	3	0x8086	0xA170	Intel High Definition Audio
0	31	4	0x8086	0xA123	SMBus Controller
0	31	5	0x8086	0xA124	SPI Controller
0	31	6	0x8086	0x15B7	Ethernet Controller NC1 (Intel i219LM)
1 [3]	00	0	0x1B4B	0x9230	SATA Host Controller (not populated)
2 [3]	00	0	0x8086	0x157B	Ethernet Controller NC2 (Intel i210IT)

1) Depends on UEFI/BIOS settings.
2) Depending on UEFI/BIOS settings different RAID modes may lead to other Device IDs.
3) Bus number can vary depending on the PCI enumeration schema implemented in UEFI/BIOS.

Local SMB/I²C Devices

The PC7-FESTIVAL contains devices that are attached to the System Management Bus (SMBus). These are the SPD EEPROMs for the on-board memory or the possibly plugged SODIMM, a general purpose serial EEPROM containing board configuration data, the supply voltage/temperature controlling device NCT7491, a set of board control and status registers as well as two general purpose, non-volatile electronic jumpers. Additional devices may be connected to the different I²C controllers of the CM238 via the *CompactPCI*® PlusIO backplane signals I²C_SCL (J1 Pin B17) and I²C_SDA (J1 Pin C17) or the mezzanine expansion connectors P-HSE2 or P-EXP.

Controller	Address	Description
SMBus	0x2C	Hardware Monitor/Memory Down Temperature Sensor (7491)
SMBus	0x2E	Board Control/Status
SMBus	0x2F	Non-volatile Electronic Jumper
SMBus	0x50 0x36/0x37	SPD EEPROM of On-board Memory 4KBit EEPROM Select Bank 0/1
SMBus	0x52 0x36/0x37	SPD EEPROM of SODIMM 4KBit EEPROM Select Bank 0/1
SMBus	0x57	General Purpose EEPROM 2KBit
I2C[0]	[1)]	P-HSE2 (Pins A22/A23), P-EXP (Pins 29/30)
I2C[1]	[1)]	CompactPCI PlusIO backplane J1 (Pins B17/C17)

1) Address depends on devices attached

Hardware Monitor NCT7491

Attached to the SMBus, the PC7-FESTIVAL is provided with the hardware monitor NCT7491. This device is capable to observe the temperatures of the board, processor cores, and on-board memory, as well as several supply voltage rails with a resolution of 10 bit. The following table shows the mapping of the voltage inputs of the NCT7491 to the corresponding supply voltages of the PC7-FESTIVAL:

Input	Source	Resolution	Register (MSB/LSB)
VCCP	Processor Core Voltage	2.93mV	0x21/0x76[3:2]
VTT	+1.0V	2.20mV	0x1E/0x1F[5:4]
+2.5V/THERM#	+1.2V	3.26mV	0x20/0x76[1:0]
VCC	+3.3V	4.29mV	0x22/0x76[5:4]
+5Vin	+5.0V	6.54mV	0x23/0x76[7:6]
+12Vin	+12.0V	15.92mV	0x24/0x77[1:0]
PECI	Core #0 absolute Temperature	1°C	0x04
PECI	Core #1 absolute Temperature	1°C	0x05
PECI	Core #2 absolute Temperature	1°C	0x06
PECI	Core #3 absolute Temperature	1°C	0x07
D1+/D1-	Memory Down absolute Temperature	0.25°C	0x25/0x77[3:2]
Local TEMP	PC7 Surface Temperature	0.25°C	0x26/0x77[5:4]

Beside the continuous measuring of temperatures and voltages the NCT7491 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value range, the NCT7491 can request an over-temperature event on GPP_D1 input of the CM238 or an interrupt via the GPP_D2 input (which may result in a system management interrupt).

Board Control and Status Registers (BCSR)

A set of board control and status registers allow to program special features on the PC7-FESTIVAL:

- Assert a full reset
- Control activity of front panel reset and power event button
- Program time-outs and trigger a watchdog
- Get access to two LEDs in the front panel
- Get power fail and watchdog status of last board reset

The register set consists of five registers located on the SMBus at Device ID=0x5c on the following addresses:

- 0xA0: CMD_CTRL0_WR: Write to Control Register 0 (Write-Only)
- 0xA1: CMD_CTRL0_RD: Read from Control Register 0 (Read-Only)
- 0xB0: CMD_STAT0_WR: Write to Status Register 0 (Write-Clear)
- 0xB1: CMD_STAT0_RD: Read from Status Register 0 (Read-Only)
- 0xB2: CMD_STAT1_WR: Write to Status Register 1 (Write-Clear)
- 0xB3: CMD_STAT1_RD: Read from Status Register 1 (Read-Only)
- 0xC1: CMD_PLDREV_RD: Read from PLD Revision Register (Read-Only)

To prevent misfunction accesses to the registers should be done by SMBus “Byte Data” commands. Further writes to read-only or reads to write-only registers should be omitted.

Write/Read Control Register 0

Write: SMBus Address 0xA0 Default after reset: 0x00

Read: SMBus Address 0xA1

Bit	Description CMD_CTRL0
7	GPLED 0=Green part of the front panel LED GP is off (Default) 1=Green part of the front panel LED GP is on
6	FPDIS 0=Enable the front panel handle switch (Default) 1=Disable the front panel handle switch
5	FERP# 0=The front panel handle switch generates a power event (Default) 1=The front panel handle switch generates a system reset
4:3	WDGT0:WDGT1 Maximum Watchdog retrigger time: 0:0 2 sec 1:0 10 sec 0:1 50 sec 1:1 250 sec
2	WDGTRG Retrigger Watchdog. Any change of this bit will retrigger the watchdog. After a system reset the watchdog is in an inactive state. The watchdog is armed on the 1st edge of this bit.
1	PGLED 0=Red part of the front panel LED PG is off (Default) 1=Red part of the front panel LED PG is blinking
0	SRES 0=Normal operation (Default) 1=A full system reset is performed

Read/Clear Status Register 0

Write: SMBus Address 0xB0
Read: SMBus Address 0xB1

Bit	Description CMD_STAT0
7	PF18S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.8S voltage regulator
6	PF10S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.0S voltage regulator
5	PF10A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.0A voltage regulator
4	PF25S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V2.5S4 voltage regulator
3	PF12S4 0=Normal operation 1=Last system reset may be caused by a power failure of the +V1.2S4 voltage regulator
2	PFVRST 0=Normal operation 1=Last system reset may be caused by a power failure of the +VCCST load switch
1	PFVRIO 0=Normal operation 1=Last system reset may be caused by a power failure of the +VCCIO voltage regulator
0	PFVRC 0=Normal operation 1=Last system reset may be caused by a power failure of the IMVP-8 voltage regulator

The bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read/Clear Status Register 1

Write: SMBus Address 0xB2
Read: SMBus Address 0xB3

Bit	Description CMD_STAT1
7	WDGARMD 0=Normal operation 1=The watchdog is armed and has to be retriggered within its time-out period
6	WDGRST 0=Normal operation 1=Last system reset may be caused by a watchdog time-out
5	WDGHT 0=Normal operation 1=The watchdog already has elapsed half of its time-out period
4	PF5PS 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5PS voltage regulator
3	PF5S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V5S voltage regulator
2	PF33L 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3LAN load switch
1	PF33A 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3A voltage regulator
0	PF33S 0=Normal operation 1=Last system reset may be caused by a power failure of the +V3.3S voltage regulator

Except of WDGHT and WDGARMD the bits in this register are sticky, i.e. their state will be kept even if a system reset occurs. To clear the bits a write to the register with arbitrary data may be performed.

Read PLD Revision Register

Write: Not allowed

Read: SMBus Address 0xC1

Bit	Description CMD_PLDREV
7:0	PLDREV Read PLD Revison Number

GPIO Usage

GPIO Usage CM238 PCH

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group A (GPP_A)				
A0	Native	IN	RCIN#	Keyboard Reset, to P-EXP Pin 13
A1-A4	Native	I/O	LPC_AD[0-3]	LPC Address/Data Lines
A5	Native	OUT	LPC_FRAME#	LPC Frame
A6	Native	IN	SERIRQ	Serialized IRQ
A7	Native	IN	PIRQA#	Not used on PC7 (pulled via resistor to +3.3V)
A8	Native	IN	CLKRUN#	Not used on PC7 (pulled via resistor to +3.3V)
A9	Native	OUT	CLKOUT_LPC0	24MHz LPC Clock, to P-EXP Pin 3
A10	Native	OUT	CLKOUT_LPC1	24MHz LPC Clock, to TPM
A11	Native	IN	PME#	Power Management Event, to P-EXP Pin 14
A12-A13	GPIO	IN	N/A	Not connected on PC7
A14	Native	OUT	N/A	Not connected on PC7
A15-A16	GPIO	IN	N/A	Not connected on PC7
A17-A19	GPIO	IN	HW_REV[0:2]	PCB Revision Code HW_REV[2:0] GPIO[19:17] 000 001 010 ... 110 111 Revision 0 1 2 6 7
A20	GPIO	OUT	SE_SYS_WP	TPM2.0 Physical Present Pin
A21-A23	GPIO	IN	N/A	Not connected on PC7
Group B (GPP_B)				
B0	GPIO	OUT	ENABLE_NC2	Enable Ethernet Controller NC2
B1-B5	GPIO	IN	N/A	Not connected on PC7
B6	Native	IN	CLKREQ1#	*CompactPCI*® Clock Request Slot 1 (J2 B12 CLKOE_1J2#_D)
B7	Native	IN	CLKREQ2#	*CompactPCI*® Clock Request Slot 2 (J2 C12 CLKOE_2J2#_D)
B8	Native	IN	CLKREQ3#	*CompactPCI*® Clock Request Slot 3 (J2 C13 CLKOE_3J2#_D)
B9	Native	IN	CLKREQ4#	*CompactPCI*® Clock Request Slot 4 (J2 C14 CLKOE_4J2#_D)
B11-B12	GPIO	IN	N/A	Not connected on PC7
B13	Native	OUT	PLTRST#	Platform Reset
B14	Native	OUT	SPEAKER	Speaker, to P-EXP Pin 39
B15-B17	GPIO	IN	N/A	Not connected on PC7
B18	GPIO	OUT	N/A	Not used on PC7, Hardware Strap to disable TCO Watchdog
B19-B21	GPIO	IN	N/A	Not connected on PC7
B22	GPIO	OUT	USB_POWEN1	USB Front Panel Right Port Power Enable
B23	GPIO	OUT	USB_POWEN2	USB Front Panel Left Port Power Enable

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group C (GPP_C)				
C0	Native	I/O	SMBCLK	SMBus Clock Line
C1	Native	I/O	SMBDATA	SMBus Data Line
C2	GPIO	IN	N/A	Not used on PC7, pulled to +3.3V
C3	Native	I/O	SML0CLK	SMLink[0] Clock Line, to Ethernet Controller NC1
C4	Native	I/O	SML0DATA	SMLink[0] Data Line, to Ethernet Controller NC1
C5	GPIO	OUT	N/A	Not connected on PC7
C6-C7	GPIO	IN	N/A	Not connected on PC7
C8	Native	IN	UART0_RXD	UART[1] RXD Line, to P-EXP Pin 25
C9	Native	OUT	UART0_TXD	UART[1] TXD Line, to P-EXP Pin 23
C10	Native	OUT	UART0_RTS#	UART[1] RTS# Line, to P-EXP Pin 24
C11	Native	IN	UART0_CTS#	UART[1] CTS# Line, to P-EXP Pin 26
C12	Native	IN	UART1_RXD	UART[2] RXD Line, to P-EXP Pin 18
C13	Native	OUT	UART1_TXD	UART[2] TXD Line, to P-EXP Pin 17
C14	Native	OUT	UART1_RTS#	UART[2] RTS# Line, to P-EXP Pin 20
C15	Native	IN	UART1_CTS#	UART[2] CTS# Line, to P-EXP Pin 27
C16	Native	I/O	I2C0_DATA	I^2C Data Line, to Connectors P-HSE2 Pin A23/P-EXP Pin 30
C17	Native	I/O	I2C0_CLK	I^2C Clock Line, to Connectors P-HSE2 Pin A22/P-EXP Pin 29
C18	Native	I/O	I2C1_DATA	I^2C Data Line, to CompactPCI PlusIO J1 Pin C17
C19	Native	I/O	I2C1_CLK	I^2C Clock Line, to CompactPCI PlusIO J1 Pin B17
C20-C23	GPIO	IN	N/A	Not connected on PC7

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group D (GPP_D)				
D0	GPIO	IN	CPCI_PS_FAL_ON#	Sense CompactPCI PlusIO Power Failure, J2 Pin C15
D1	GPIO	IN	PM_MEMTS#	Memory Thermal Sensor Event
D2	GPIO	IN	HM_INT#	Hardware Monitor NCT7491 Alert Line
D3-D8	GPIO	IN	N/A	Not connected on PC7
D9	GPIO	IN	GP_JUMP#	Reset UEFI/BIOS Setup to Factory Defaults, Jumper J-GP
D10	GPIO	IN	CPCI_SYSEN#	Sense CompactPCI PlusIO System Slot Enable, J2 Pin C2
D11	GPIO	OUT	GP_LED_RED	General Purpose Red LED Control (via PLD)
D12-D20	GPIO	IN	N/A	Not connected on PC7
D21	GPIO	OUT	SE_SYS_WP	General Purpose Serial EEPROM Write Protection
D22	GPIO	OUT	PPSM_EN	Connect IEEE 1588 PPS/PPM to J-GP and CompactPCI PlusIO J2 LO: Isolate PPS/PPM Signals HI: Connect PPS/PPM to J-GP/P1
D23	GPIO	IN	N/A	Not connected on PC7
Group E (GPP_E)				
E0	Native	IN	SATA#PCIE12	P-HSE1 HS Lanes 1/2 Configuration LO: Configured as SATA HI: Configured as PCIe
E1	Native	IN	SATA#PCIE12	Shorted to GPP_E0
E2	Native	IN	SATA#PCIE34	P-HSE1 HS Lanes 3/4 Configuration LO: Configured as SATA HI: Configured as PCIe
E3-E7	GPIO	IN	N/A	Not connected on PC7
E8	Native	OUT	SATALED#	Signal PCH SATA activity via green HD LED in Front Panel (to PLD)
E9	Native	IN	USB_FP_OC1#	USB Front Panel Right Port Overcurrent Detect
E10	Native	IN	USB_FP_OC2#	USB Front Panel Left Port Overcurrent Detect
E11	Native	IN	USB_HSE1_OC#	Overcurrent Detect on any P-HSE1 USB Port
E12	GPIO	IN	N/A	Not connected on PC7

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Group F (GPP_F)				
F0	Native	IN	SATA#PCIE34	Shorted to GPP_E2
F1-F9	GPIO	IN	N/A	Not connected on PC7
F10	Native	OUT	SGPIO_CLOCK	*CompactPCI* PlusIO GPIO Bus CLOCK (J2 D14 SATA_SCL)
F11	Native	OUT	SGPIO_LOAD	*CompactPCI* PlusIO GPIO Bus LOAD (J2 E13 SATA_SL)
F12	GPIO	IN	SGPIO_IN	*CompactPCI* PlusIO GPIO Bus DATAIN (J2 D12 SATA_SDI)
F13	Native	OUT	SGPIO_OUT	*CompactPCI* PlusIO GPIO Bus DATAOUT (J2 D13 SATA_SDO)
F14-F23	GPIO	IN	N/A	Not connected on PC7
Group G (GPP_G)				
G0-G18	GPIO	IN	N/A	Not connected on PC7
G19	Native	IN	SMI#	Connected to P-EXP SMI# Signal (Pin 15)
G20-G23	GPIO	IN	BOARD_CFG	Board Configuration Jumpers BOARD_CFG[0:3]
Group H (GPP_H)				
H0	Native	IN	N/A	Not connected on PC7
H1	Native	IN	N/A	Not connected on PC7
H2	Native	IN	N/A	Not connected on PC7
H3	Native	IN	PCIE_CLK_REQ9#	Ethernet Controller NC1 Clock Request
H4-H11	GPIO	IN	N/A	Not connected on PC7
H12	GPIO	OUT	N/A	Not connected on PC7
H13-H23	GPIO	IN	N/A	Not connected on PC7
Group I (GPP_I)				
I0	Native	IN	DDPB_HPD1	DisplayPort Front Panel Upper Port Hot Plug Detect
I1	Native	IN	DDPB_HPD2	DisplayPort Front Panel Lower Port Hot Plug Detect
I2	Native	IN	DDPB_HPD3	DisplayPort P-HSE2 Port Hot Plug Detect
I3	GPIO	IN	N/A	Not connected on PC7
I4	GPIO	IN	N/A	Not used on PC7 (pulled via resistor to GND)
I5	Native	OUT	DDPB_CTRLCLK	DisplayPort Front Panel Upper Port DDC_CLK
I6	Native	I/O	DDPB_CTRLDTA	DisplayPort Front Panel Upper Port DDC_DATA
I7	Native	OUT	DDPC_CTRLCLK	DisplayPort Front Panel Lower Port DDC_CLK
I8	Native	I/O	DDPC_CTRLDTA	DisplayPort Front Panel Lower Port DDC_DATA
I9	Native	OUT	DDPD_CTRLCLK	DisplayPort P-HSE2 Port DDC_CLK
I10	Native	I/O	DDPD_CTRLDTA	DisplayPort P-HSE2 Port DDC_DATA

GPIO Usage CM238 PCH				
GPIO	USAGE	DIR	Function	Description
Deep Sleep Well Group (GDP)				
0	Native	IN	BATLOW#	Not used on PC7 (pulled via resistor to +3.3V)
1	Native	IN	ACPRESENT	Not used on PC7 (pulled via resistor to +3.3V)
2	Native	IN	LAN_WAKE#	Connected to Ethernet Controller NC1 LAN_WAKE#
3	Native	IN	PWRBTN#	Power Button Event, connected to PLD
4	Native	OUT	SLP_S3#	Power Management Signal, connected to PLD
5	Native	OUT	SLP_S4#	Power Management Signal, connected to PLD
6	GPIO	IN	N/A	Not connected on PC7
7	GPIO	OUT	N/A	Not connected on PC7
8	Native	OUT	SUSCLK	Buffer Clock from RTC, connected to a Test Point
9	Native	OUT	SLP_WLAN#	Not connected on PC7
10	Native	OUT	SLP_S5#	Power Management Signal, connected to PLD
11	Native	OUT	ENABLE_NC1	Enable Ethernet Controller NC1

All GPIO groups are sourced by +3.3V supply active in power states S0-S5.

Configuration Jumpers

Loading UEFI/BIOS Setup Defaults/IEEE 1588 Pulse per Second (J-GP)

The jumper J-GP may be used to reset the UEFI/BIOS configuration settings to a default state. The UEFI/BIOS on PC7-FESTIVAL stores most of its settings in an area within the UEFI/BIOS flash, e.g. the actual boot devices. Using the jumper J-GP is only necessary, if it is not possible to enter the setup of the UEFI/BIOS. To reset the settings mount a jumper on J-GP and perform a system reset. As long as the jumper is stuffed the UEFI/BIOS will use the default configuration values after any system reset. To get normal operation again, the jumper has to be removed.

There is also an alternate function available on J-GP. Pin 1 of this jumper carries a Pulse per Second (PPS) signal according the IEEE 1588 specification when enabled by UEFI/BIOS settings. A wire may be connected to trigger events on external devices.

Note: The PPS signal can be gripped at the CompactPCI® PlusIO connector J2 pin D14.

J-GP

J-GP	Function
Jumper removed [1)]	Normal operation
Jumper installed	UEFI/BIOS configuration reset performed

1) This setting is the factory default

Manufacturer Mode Jumper (J-MFG)

The jumper J-MFG is used to bring the board into the manufacturer mode. This is necessary only on board production time and should not used by customers. For normal operation the jumper should be removed. The pin header J-MFG is not stuffed on the PC7-FESTIVAL by default.

J-MFG

J-GP	Function
Jumper removed [1)]	Normal operation
Jumper installed	Entering Manufacturer Mode

1) This setting is the factory default

RTC Reset (J-RTC)

The jumper J-RTC may be used to reset certain register bits of the battery backed RTC core within the PCH CM238. This can be necessary under rare conditions (e.g. battery undervoltage), if the CPU fails to enter the UEFI/BIOS POST after power on.

Note: The installing of jumper J-RTC will neither set UEFI/BIOS Setup to EKF Factory Defaults nor resets the time and date register values of the RTC (Real Time Clock). To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of J-RTC for about 1 sec. Thereafter reinstall the board to the system and switch on the power. The pin header J-RTC is not stuffed on the PC7-FESTIVAL by default.

Note: It is important to accomplish the RTC reset while the board has no power.

J-RTC

J-GP	Function
Jumper removed [1)]	Normal operation
Jumper installed	RTC reset performed

1) This setting is the factory default

Connectors

Caution: Some of the internal connectors provide operating voltage (3.3V, 5V and 12V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are short circuit protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors

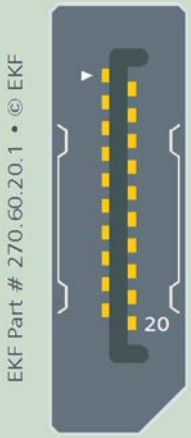
The basic PC7-FESTIVAL front panel connectors are comprised of each two DisplayPort, USB3 Type-A and RJ45 Ethernet jacks. If low profile mezzanine modules are employed, one or two Type-C receptacles may be available for front I/O in addition. Documentation on the Type-C connectors is not provided in this manual - please refer to the particular mezzanine module in use.

For 8HP/12HP front panel width assemblies together with a side card e.g. PCZ-NVM please refer to the particular side card documentation.

DisplayPort Connectors

The Intel graphics processing unit (GPU) on the PC7-FESTIVAL processor carrier card incorporates up to three external DisplayPort video channels. Two video outputs are available via the CPU card front panel (standard DisplayPort receptacles, reverse mount). A third DP signal channel is passed across the HSE2 mezzanine connector for optional use on a mezzanine card.

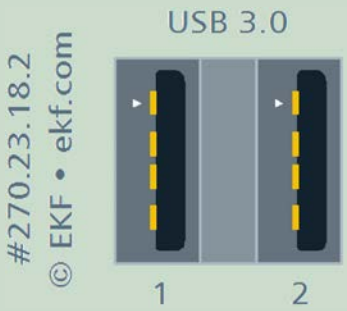
Independent operation of multiple displays (e.g. Windows® Expanded Desktop) is enabled by the Intel graphics drivers.

DP1 & DP2 • DisplayPort Video Standard DisplayPort Receptacles (Reverse Mount Type) 20-lead (270.60.20.1)				
	1	LANE0(P)	2	GND
	3	LANE0(N)	4	LANE1(P)
	5	GND	6	LANE1(N)
	7	LANE2(P)	8	GND
	9	LANE2(N)	10	LANE3(P)
	11	GND	12	LANE3(N)
	13	CONFIG1	14	CONFIG2 (GND)
	15	AUX(P)	16	GND
	17	AUX(N)	18	Hot Plug Detect
	19	Power Return	20	Power +3.3V 0.5A [1)]

1) Sourced via electronic power switch (back driving protected), maximum current for short circuit detection 1.5A. Voltage supply active only in power state S0.

USB Connectors

The Intel® CM238 Platform Controller Hub incorporates a four-port USB 3.0 xHCI host controller. Two ports are directly available on the PC7-FESTIVAL front panel (type A receptacle), for attachment of external USB devices.

P-USB • Dual USB 3.0 Receptacle USB 3.0 dual type A receptacle, stacked, 18-position		
	1	VBUS +5V, 1.5A max [1]
	2	USB D-
	3	USB D+
	4	GND
	5	SS RX-
	6	SS RX+
	7	GND
	8	SS TX-
	9	SS TX+

1) +5V via 1.5A current-limited electronic power switch. The voltage is active in power states S0-S5 and may be switched off by software independently for each port.

Ethernet Connectors

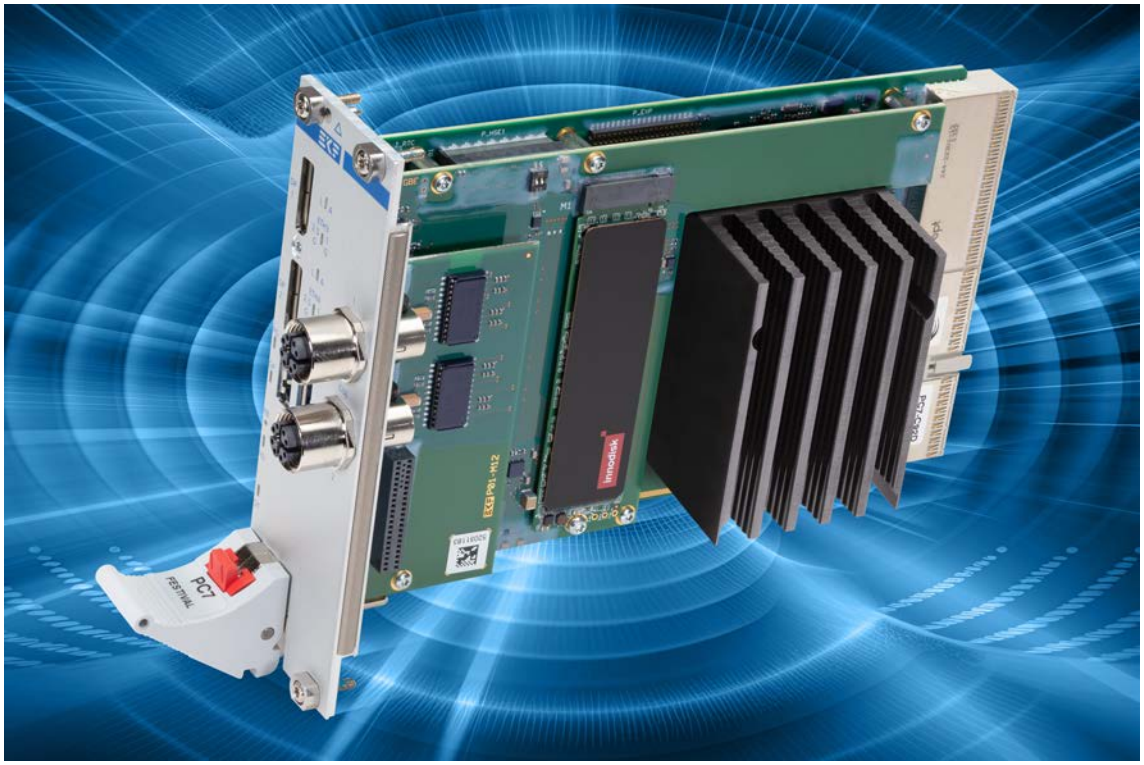
Gigabit Ethernet Ports 1/2 (P-ETH, RJ-45)			
 270.02.08.5	Port 1	1	NC1_MDX0+
		2	NC1_MDX0-
		3	NC1_MDX1+
		4	NC1_MDX2+
		5	NC1_MDX2-
		6	NC1_MDX1-
		7	NC1_MDX3+
		8	NC1_MDX3-
	Port 2	1	NC2_MDX0+
		2	NC2_MDX0-
		3	NC2_MDX1+
		4	NC2_MDX2+
		5	NC2_MDX2-
		6	NC2_MDX1-
		7	NC2_MDX3+
		8	NC2_MDX3-

The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established. The upper green/yellow dual-LED signals the link speed 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off.

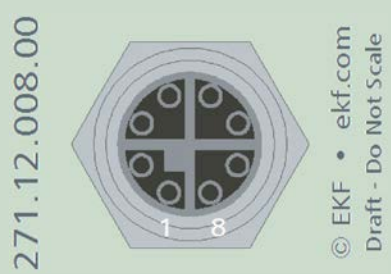
Option M12 X-Coded Ethernet Receptacles

As an ordering option, the PC7-FESTIVAL RJ45 jacks can be replaced by M12 X-coded receptacles. A small mezzanine module (P01-M12) is soldered to the RJ45 footprint, resulting in an 8HP front panel assembly. The P01-M12 can be combined with any low profile module available for the PC7-FESTIVAL, i.e. S48-SSD, C48-M2, P82-GBE.

PC7 w. P01 8HP Assembly


PC7
FESTIVAL
Innodisk


GbE
USB
PC7
FESTIVAL

M12 X-Coded Front Panel I/O Receptacles Gigabit Ethernet • 271.12.008.20 • M12-X Flush-type socket			
	Ports 1-2	1	MDX0+
		2	MDX0-
		3	MDX1+
		4	MDX1-
		5	MDX3+
		6	MDX3-
		7	MDX2-
		8	MDX2+

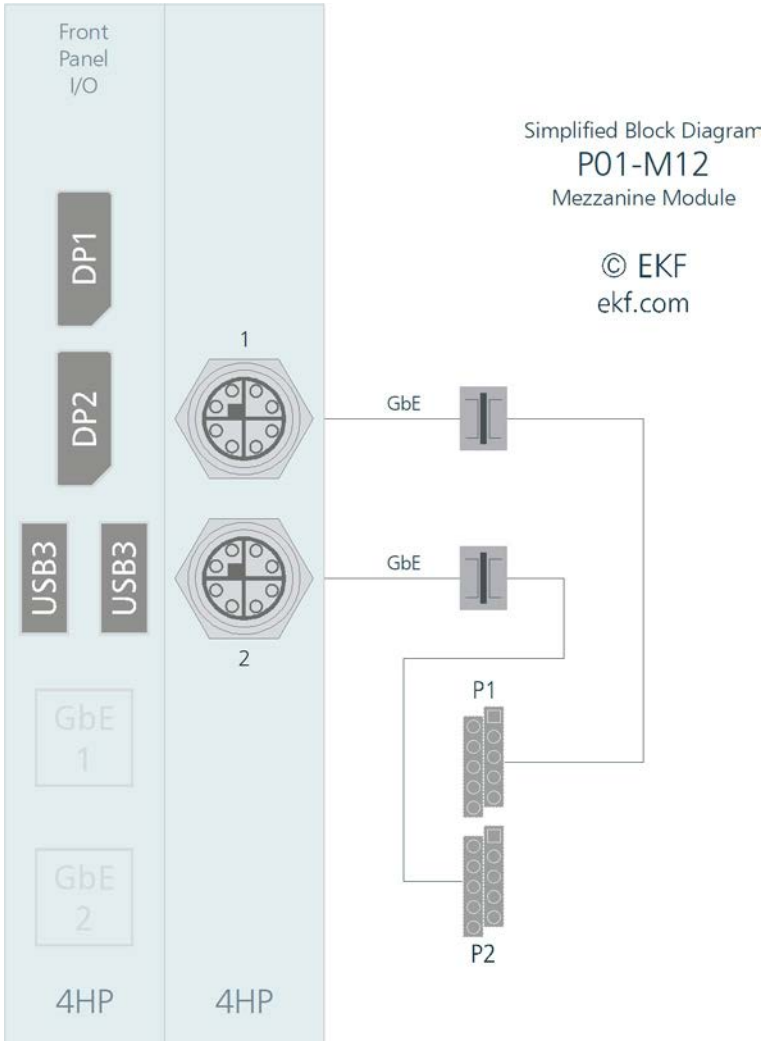
The pin numbers of an M12 X-coded connector do not reflect the RJ45 Gigabit Ethernet signal assignment. For cross-over patch cables M12 to RJ45 please refer to the table below.

M12 X	Signal Colors T568B	RJ45
1	MDX0+ white/orange	1
2	MDX0- orange	2
3	MDX1+ white/green	3
4	MDX1- green	6
5	MDX3+ white/brown	7
6	MDX3- brown	8
7	MDX2- white/blue	5
8	MDX2+ blue	4

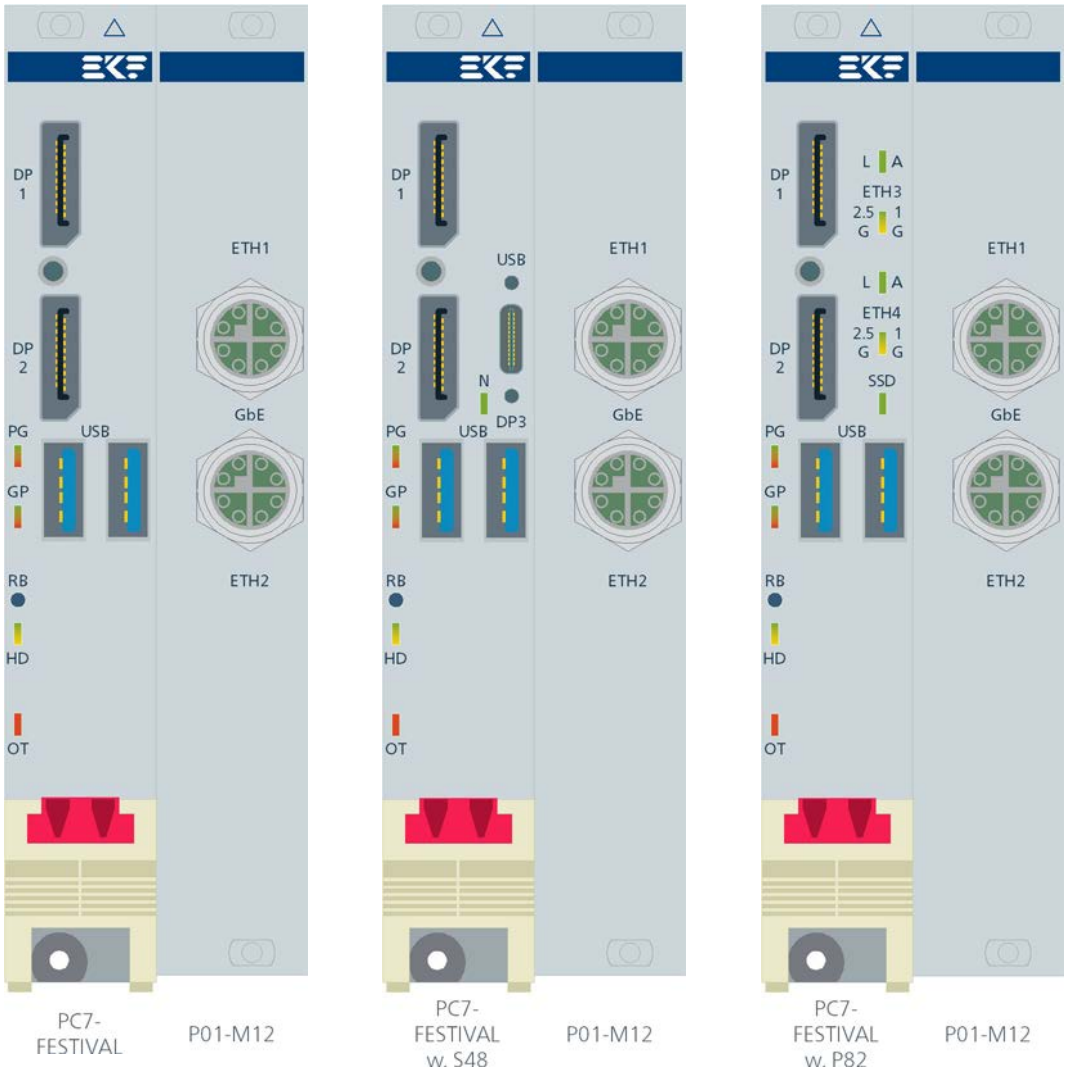
Suitable industrial Gigabit Ethernet M12 cable assemblies can be ordered from EKF, or directly from well-known cable and connector manufacturers e.g. Metz, Phoenix, Escha and many others.

Ordering Information Cable Assemblies
Gigabit Ethernet cable M12 to M12: #271.14.008.xx (xx=length/meter)
Gigabit Ethernet cable M12 to RJ-45: #271.15.008.xx (xx=length/meter)

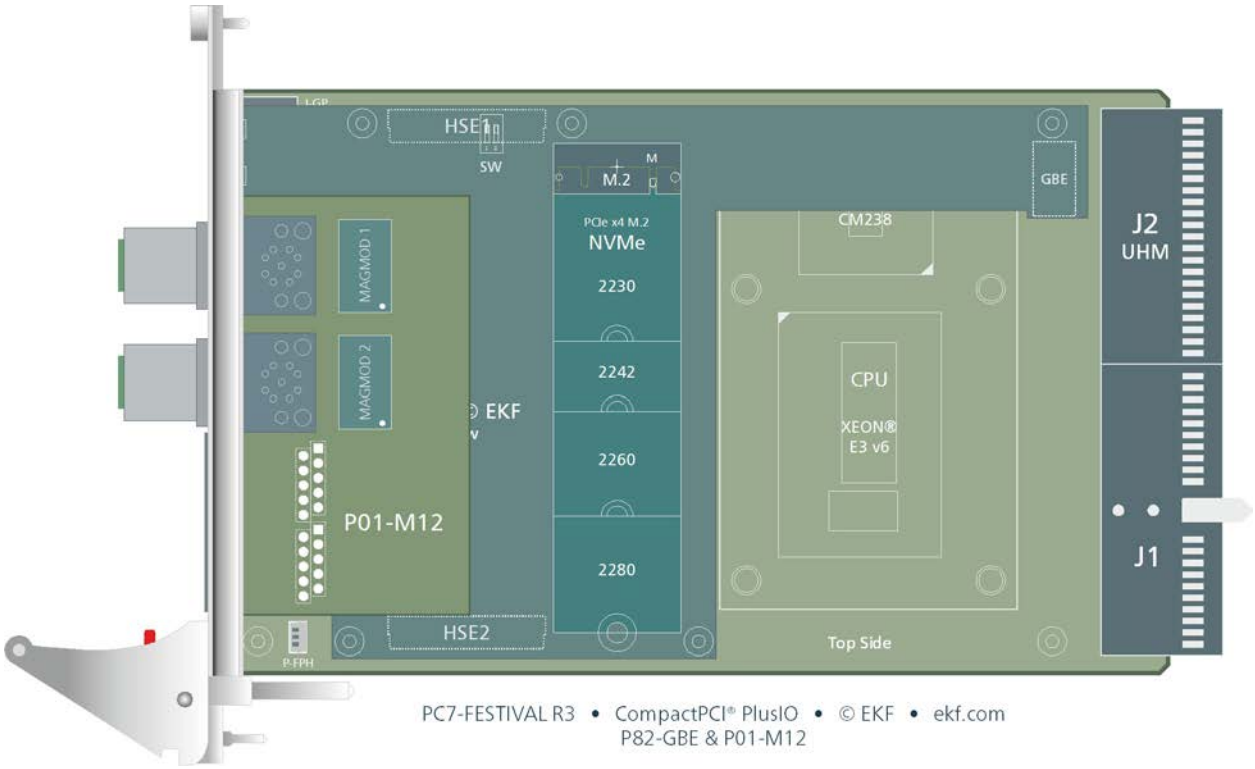

DP
J-GP
P-MEZ
EXP
M.2-2
2230
2242
2260
2280
PCH
CM238
CPU
XEON®
E3 v6
J2
UHM
J1
MAGMOD 1
MAGMOD 2
C48-M2 © EKF
P01-M12
P-FPH
Top Side
PC7-FESTIVAL • CompactPCI® PlusIO • © EKF • ekf.com


Front
Panel
I/O
DP1
DP2
USB3
USB3
GbE
1
GbE
2
4HP
4HP
1
2
GbE
GbE
P1
P2
Simplified Block Diagram
P01-M12
Mezzanine Module
© EKF
ekf.com

The P01-M12 connector option can be combined with low profile mezzanine modules, e.g. S48-SSD or P82-GBE.



PC7-FESTIVAL • CompactPCI® PlusIO • © EKF • ekf.com
with S48-SSD & P01-M12



PC7-FESTIVAL R3 • CompactPCI® PlusIO • © EKF • ekf.com
P82-GBE & P01-M12

Mezzanine Connectors

Up to four connectors are available for PC7-FESTIVAL mezzanine expansion. Two high speed signal connectors (HSE1, HSE2) and in addition a legacy I/F connector (EXP) are populated on top of the CPU board. From PCB Rev.3 off, there is an optional GBE mezzanine connector for use with the P82-GBE low profile module.

EKF offers low profile mezzanine modules which fit into the 4HP envelope of the CPU carrier card, with varying B2B clearance from 9.5mm to 10.8mm, and also side cards for additional 4HP mounting pitch (8HP in total assembly, 18.7mm B2B). The female connector EXP is identically populated on carrier and mezzanine and requires a suitable pin header (stacker) as contact element between carrier and mezzanine in addition. The HSE1/HSE2 connectors of carrier and mezzanine are female (CPU) and male (mezzanine) pairs, selected to match the individual B2B height requirements:

HSE1/HSE2 Mezzanine Connectors	
Mezzanine Series, B2B	Connector
CPU Carrier	8mm female ERNI Microspeed 275.90.08.068.01
C4*, B2B 9.5mm	Supplement 1mm male connector for nominal height 9mm
P82, S2*, S4*, B2B 10.0mm	Supplement 2mm male connector for nominal height 10mm
S6*, S8*, B2B 10.8mm	Supplement 2mm male connector for nominal height 10mm
PC*, SC* side card, B2B 18.7mm	Supplement 8mm male connector for nominal height 18mm

Series	Board to Board Space	HSE1	HSE2	GBE	M.2 Profile	Type-C Front I/O	Ethernet Backplane	Side Card Option 8HP (HSE2)
C4x	9.5mm	SATA x4 3)	1)	○	S1 - S5 D1 - D4	○	○	○
P82	10.0mm	PCIe x4, USB3	PCIe 4x1	2 x 2.5GbE	S1 - S5 D1 - D4	○	J2	○
S2x	10.0mm	PCIe x4, USB3	2)	○	S1 - S5 D1 - D4	✓	○	✓
S4x	10.0mm	PCIe x4, USB3	PCIe 4x1, DP	○	S1 - S5 D1 - D4	✓	○	○
S6x	10.8mm	PCIe x2, SATA x2, USB3	2)	○	S1 - S5	○	○	✓
S8x	10.8mm	PCIe x4, USB3	PCIe 4x1, DP	○	S1 - S5	○	P6	○

1) HSE2 covered by mezzanine PCB - not usable for additional 8HP side card
2) HSE2 recessed on mezzanine PCB - available for additional 8HP side card (option)
3) Two SATA ports in use on mezzanine (C47: SATA 2/3, C48: SATA 1/2)

✓ Feasible (option)
○ Not scheduled or infeasible

Popular M.2 component heights:
D3 Double sided M.2 (top 1.5mm, bottom 1.35mm)
S3 Single sided M.2 (top 1.5mm)
For full nomenclature please refer to the PCI Express M.2 Mechanical Specification chapter 2.2

Related Information	
New Mezzanine Connectors Explained	www.ekf.com/s/mezzanine_connectors.pdf

High Speed Expansion P-HSE1				
	CFG_12 [5]	a1	b1	CFG_34 [5]
	1_SATA_PCIE_TXP	a2	b2	3_SATA_PCIE_TXP
	1_SATA_PCIE_TXN	a3	b3	3_SATA_PCIE_TXN
	GND	a4	b4	GND
	1_SATA_PCIE_RXN	a5	b5	3_SATA_PCIE_RXN
	1_SATA_PCIE_RXP	a6	b6	3_SATA_PCIE_RXP
	GND	a7	b7	GND
	2_SATA_PCIE_TXP	a8	b8	4_SATA_PCIE_TXP
	2_SATA_PCIE_TXN	a9	b9	4_SATA_PCIE_TXN
	GND	a10	b10	GND
	2_SATA_PCIE_RXN	a11	b11	4_SATA_PCIE_RXN
	2_SATA_PCIE_RXP	a12	b12	4_SATA_PCIE_RXP
	GND	a13	b13	GND
	1_USB2_P	a14	b14	2_USB3_TXP
	1_USB2_N	a15	b15	2_USB3_TXN
	GND	a16	b16	GND
	2_USB2_P	a17	b17	2_USB3_RXP
	2_USB2_N	a18	b18	2_USB3_RXN
	GND	a19	b19	GND
	1_2_USB_OC# [6]	a20	b20	PCIE_CLK_P
	PLTRST#	a21	b21	PCIE_CLK_N
	+3.3VS [1]	a22	b22	+5VS [1]
	+3.3VS [1]	a23	b23	+5VS [1]
	+3.3VA [3]	a24	b24	+5VA [2]
	+12VA [4]	a25	b25	+12VA [4]

1) Power rail switched on in S0 state only
2) Power rail passed through from J1 backplane connector +5V
3) Power rail passed through from J1 backplane connector +3.3V (if supported from power supply)
4) Power rail passed through from J1 backplane connector +12V (not usually supported from power supply)
5) CFG_12/CFG_34: GND configures to SATA, OPEN or HIGH configures to PCIe
6) Signal is 3.3V tolerant only

P-HSE2

High Speed Expansion P-HSE2				
	1_PCIE_TXP	a1	b1	3_PCIE_TXP
	1_PCIE_TXN	a2	b2	3_PCIE_TXN
	GND	a3	b3	GND
	1_PCIE_RXN	a4	b4	3_PCIE_RXN
	1_PCIE_RXP	a5	b5	3_PCIE_RXP
	GND	a6	b6	GND
	2_PCIE_TXP	a7	b7	4_PCIE_TXP
	2_PCIE_TXN	a8	b8	4_PCIE_TXN
	GND	a9	b9	GND
	2_PCIE_RXN	a10	b10	4_PCIE_RXN
	2_PCIE_RXP	a11	b11	4_PCIE_RXP
	GND	a12	b12	GND
	DP_LANE0_P	a13	b13	DP_LANE2_P
	DP_LANE0_N	a14	b14	DP_LANE2_N
	GND	a15	b15	GND
	DP_LANE1_P	a16	b16	DP_LANE3_P
	DP_LANE1_N	a17	b17	DP_LANE3_N
	GND	a18	b18	GND
	PCIE_CLK_P	a19	b19	DP_AUX_P
	PCIE_CLK_N	a20	b20	DP_AUX_N
	GND	a21	b21	DP_CFG1
	I2C_SCL [1)]	a22	b22	DP_HPD
	I2C_SDA [1)]	a23	b23	PLTRST#
	+5VA *(+12VA)* [2)]	a24	b24	+5VA *(+12VA)* [2)]
	+5VA *(+12VA)* [2)]	a25	b25	+5VA *(+12VA)* [2)]

1) Connected to CM238 PCH I²C Bus Controller 0, 3.3V tolerant only
2) Power rail passed through from J1 backplane connector (+5V by default, +12V stuffing option)

PCIe link width configurable via recent UEFI/BIOS & ME:
Setup (F2): Advanced -> PCI Configuration -> PCH PCI Express Configuration -> Select Link Width of PCH PCIe Controller 1-5
Available options: No override (default), 4x1, 2x2, 1x2+2x1 and 1x4

P-EXP

P-EXP • Expansion Board Interface (LPC/HD-Audio/UART) 1.27mm Socket 2 x 20 (276.53.040.01)				
	GND	1	2	+3.3VS [1]
	CLK_24MHZ *(CLK_33MHz)*	3	4	PLTRST#
	LPC_AD0	5	6	LPC_AD1
	LPC_AD2	7	8	LPC_AD3
	LPC_FRAME#	9	10	NC *(LPC_DRQ#)*
	GND	11	12	+3.3VS [1]
	SERIRQ	13	14	PME#
	SMI#	15	16	CLK_14MHZ
	2_UART_TXD *(FWH_ID0)*	17	18	2_UART_RXD *(FWH_INIT#)*
	RCIN# [4] *(KBD_RST#)*	19	20	2_UART_RTS# *(A20GATE)*
	GND	21	22	+5VS [1]
	1_UART_TXD *(2_USB2_N)*	23	24	1_UART_RTS# *(1_USB2_N)*
	1_UART_RXD *(2_USB2_P)*	25	26	1_UART_CTS# *(1_USB2_P)*
	2_UART_CTS# *(USB2_OC#)*	27	28	XDP_RESET# [5]
	I2C_SCL [3]	29	30	I2C_SDA [3]
	GND	31	32	+5VS [1]
	HDA_SDOUT	33	34	HDA_SDIN0
pin orientation shows CPU carrier board top view	HDA_RST#	35	36	HDA_SYNC
	HDA_BITCLK	37	38	HDA_SDIN1
	SPEAKER	39	40	+12VA [2]

1) Power rail switched on in S0 state only
2) Power rail passed through via 0R from J1 backplane connector
3) Connected to CM238 PCH I²C Bus Controller 0
4) Connected to CM238 PCH pin RCIN#/GPP_A0
5) Connected to debug port reset logic in order to force hardware reset
6) Signals are 3.3V tolerant only

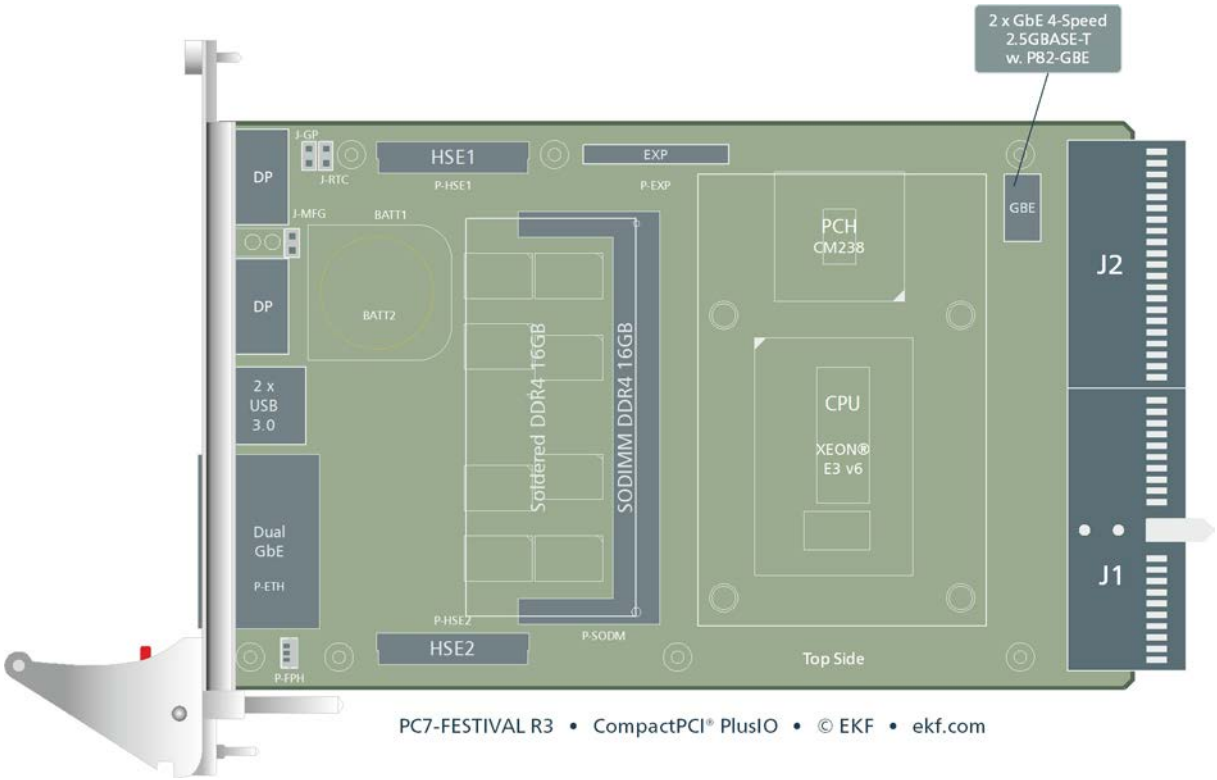
The UART pins of the P-EXP connector allow dual use - either serial I/F (native usage), or GPIO for custom specific application. Alternate 1: 1 x UART, 4 x GPIO, alternate 2: 8 x GPIO

P-GBE

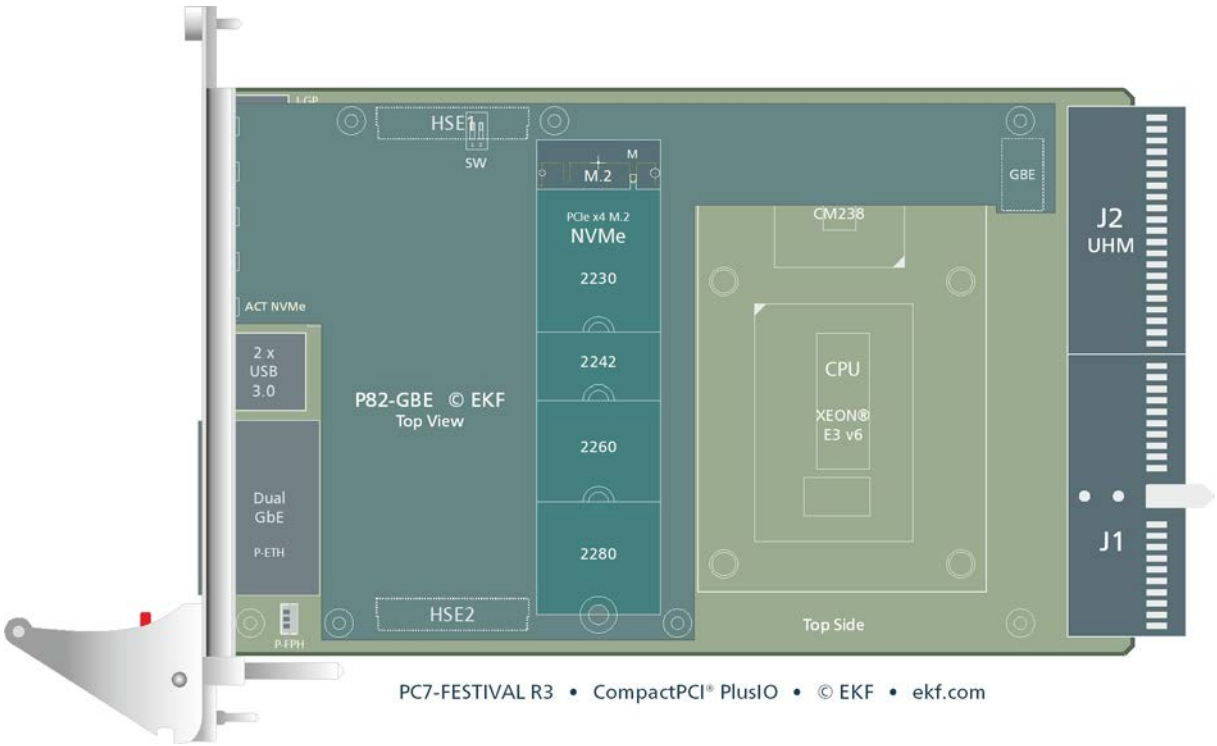
This optional connector is only used for an assembly of the PC7-FESTIVAL CPU card and the P82-GBE low profile module, for passing two ethernet ports from the mezzanine module to the backplane connector J2 on the CPU carrier card.

GBE • Expansion Connector for CompactPCI® PlusIO Backplane Ethernet Zero8 2x10 pos low profile height 1.15mm plug 275.92.01.020.51 Used on CPU card PC7-FESTIVAL from Rev. 2022 off for signal names refer to J2 backplane connector according to the CompactPCI® PlusIO specification			
1_ETH_A+	A1	B1	1_ETH_B+
1_ETH_A-	A2	B2	1_ETH_B-
GND	A3	B3	GND
1_ETH_C+	A4	B4	1_ETH_D+
1_ETH_C-	A5	B5	1_ETH_D-
2_ETH_A+	A6	B6	2_ETH_B+
2_ETH_A-	A7	B7	2_ETH_B-
GND	A3	B8	GND
2_ETH_C+	A9	B9	2_ETH_D+
2_ETH_C-	A10	B10	2_ETH_D-

P-GBE is not available with PCB revision 2. However, PCB revision 2 will remain also in production unchanged for existing projects.



GBE Connector for J2 Rear I/O Dual GbE w. P82-GBE Low Profile Mezzanine Module



Pin Headers & Debug

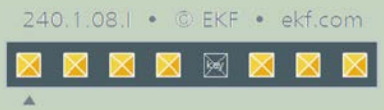
Front Panel Handle Microswitch Header P-FPH

The jumper P-FPH is used for attachment of an external SPDT switch. By default, P-FPH is connected across a short cable harness to a microswitch, which is integrated into the PC7-FESTIVAL front panel handle (ejector lever). The switch performs a power button event (e.g. system shutdown) by short-circuiting the pins 1 and 3 of P-FPH when activated (hold unlock button of front panel handle depressed momentarily).

P-FPH		
		
1	black	Microswitch Pole (Common), Wired to PLD
2	red	Microswitch Throw - F/P Handle Locked Position, NC
3	yellow	Microswitch Throw - F/P Handle Unlocked Position, Wired to GND

PLD Programming Header P-ISP

The PC7-FESTIVAL is provided with a powerful PLD (in-System Programmable Logic Device) which replaces legacy glue logic. The programming header P-ISP is not stuffed (in use for manufacturing only). Its footprint is situated at the bottom side of the board.

P-ISP	
	
1	+3.3V
2	TDO
3	TDI
4	*NC*
5	*KEY*
6	TMS
7	GND
8	TCK

Processor Debug Header P-XDP

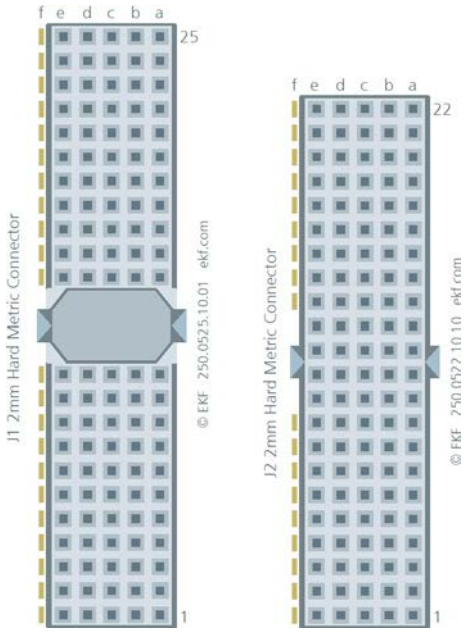
The PC7-FESTIVAL may be equipped with a 60-position processor debug header for hard- and software debugging (specified by Intel® as XDP-60 Pin Platform Connection). The connector is suitable for installation of a flat cable, in order to attach an JTAG debugger (emulator) such as the Intel® ITP-XDP3.

The header P-XDP would be mounted on the PCB bottom side. Since its heights is with 5mm much higher than the allowed 2.1mm it is not stuffed by default.

P-XDP Processor Debug Connector			
1	XDP_Pin#1	GND	2
3	OBSFN_A0	OBSFN_C0	4
5	OBSFN_A1	OBSFN_C1	6
7	GND	GND	8
9	OBSDATA_A0	OBSDATA_C0	10
11	OBSDATA_A1	OBSDATA_C1	12
13	GND	GND	14
15	OBSDATA_A2	OBSDATA_C2	16
17	OBSDATA_A3	OBSDATA_C3	18
19	GND	GND	20
21	OBSFN_B0	OBSFN_D0	22
23	OBSFN_B1	OBSFN_D1	24
25	GND	GND	26
27	OBSDATA_B0	OBSDATA_D0	28
29	OBSDATA_B1	OBSDATA_D1	30
31	GND	GND	32
33	OBSDATA_B2	OBSDATA_D2	34
35	OBSDATA_B3	OBSDATA_D3	36
37	GND	GND	38
39	HOOK0	*HOOK4*	40
41	HOOK1	*HOOK5*	42
43	VCCOBS_AB	VCCOBS_CD	44
45	*HOOK2*	HOOK6	46
47	HOOK3	HOOK7	48
49	GND	GND	50
51	*XDP_SDA*	XDP_TDO	52
53	*XDP_SCL*	XDP_TRST#	54
55	XDP_TCK1	XDP_TDI	56
57	XDP_TCK0	XDP_TMS	58
59	GND	XDP_PRESENT#	60

Backplane Connectors

The backplane connector suite is comprised of two hard metric 2.0mm connectors. While the J1 connector is compliant to CompactPCI® PICMG® 2.0, the J2 connector pin assignment follows an enhancement specification named CompactPCI® PlusIO PICMG® 2.30. This allows to combine classic CompactPCI® peripheral cards (32bit PCI) and modern CompactPCI® Serial cards according to PICMG® CPCI-S.0 on a common hybrid backplane.



CompactPCI J1

J1	A	B	C	D	E
25	5V	REQ64# [2]	ENUM# [1]	3.3V [9]	5V
24	AD1	5V	V(I/O)	AD0	ACK64# [2]
23	3.3V [9]	AD4	AD3	5V	AD2
22	AD7	GND	3.3V [9]	AD6	AD5
21	3.3V [9]	AD9	AD8	M66EN [7]	C/BE0#
20	AD12	GND	V(I/O)	AD11	AD10
19	3.3V [9]	AD15	AD14	GND	AD13
18	SERR# [1]	GND	3.3V [9]	PAR	C/BE1#
17	3.3V [9]	IPMB SCL [3]	IPMB SDA [3]	GND	PERR# [1]
16	DEVSEL# [1]	GND	V(I/O)	STOP# [1]	LOCK# [1]
15	3.3V [9]	FRAME# [1]	IRDY# [1]	BD_SEL# [6]	TRDY# [1]
14	KEY AREA (not keyed)				
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V [9]	AD20	AD19
9	C/BE3#	NC *IDSEL*	AD23	GND	AD22
8	AD26	GND	V(I/O)	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ# [1]	GND	3.3V [9]	CLK	AD31
5	*BRSVP1A5* [4]	*BRSVP1B5* [4]	RST#	GND	GNT#
4	IPMB PWR (+5V) [3]	GND *HEALTHY#*	V(I/O)	INTP [1]	INTS [1]
3	INTA# [1]	INTB# [1]	INTC# [1]	5V	INTD# [1]
2	*TCK* [4]	5V	*TMS* [4]	*TDO* [4]	*TDI* [4]
1	5V	-12V [5]	*TRST#* [4]	+12V [8]	5V

signals marked grey/italic are not connected

1) Various PCI control signals pulled up with 1kOhm to V(I/O). This value is specified for +5V V(I/O) but works as well with +3.3V V(I/O) under all environments which have been tested by EKF. On request, 2.7kOhm P/U resistors can be stuffed.

2) REQ64# and ACK64# not used on PC7-FESTIVAL, though pulled up with 1kOhm to V(I/O).

3) IPMB SCL and SDA connected to CM238 PCH I^2C port 1 via level shifter, pulled up with 1k to J1 pin A4 IPMB_PWR (+5V). IPMB_PWR can be sourced externally, and is also supplied by the PC7-FESTIVAL across a Schottky diode.

4) All JTAG pins are NC since discouraged by CPCI specification Rev. 3.0

5) -12V connected to a decoupling capacitor only and not used on PC7-FESTIVAL

6) BD_SEL# connected to PLD input, however not in logical use by default

7) M66EN is detected by the PCI bridge in order to allow either 66MHz PCI backplane operation, or when pulled low (by peripheral board) forces 33MHz clock.
Note: The PCI bridge can be setup also for 50MHz and 25MHz on customer request (resistor stuffing option). When operating in 66MHz (50MHz) a V(I/O) voltage of +3.3V is mandatory.

8) +12V passed through to mezzanine connectors P-HSE and P-EXP, not required for PC7-FESTIVAL basic operation

9) The 3.3V pins can be sourced by the PC7-FESTIVAL itself, for +5V only power supply designs (consider power 3.3V power requirements of peripheral boards).

CompactPCI J2 (PlusIO)

This connector was originally a high speed 3M UHM connector, suitable for Gigabit Serial I/O. Refer also to PICMG® 2.30 CompactPCI® PlusIO Specification. Meanwhile this connector had to be replaced by the CompactPCI® 2.0 classic J2 hard metric connector, due to an obsolescence of the 3M. This may reduce high speed backplane transfer in particular applications (PCIe® Gen1 2.5GT/s, SATA 1.5Gbps). This does not affect peripherals attached via the P-HSE mezzanine connector.

J2 UHM (Top)
J1 (Bottom)

EKF has tested successfully also PCIe® Gen2 5GT/s and SATA 6Gbps over the backplane in sample applications, but cannot guarantee this data rate under any conditions. Other devices attached and other backplane brands/types in use may cause a different result. For optimum reliability, the CM238 PCH SATA controller will be initialized at 3Gbps by default. With respect to the optional P82-GBE mezzanine, the I226 controller maximum data rate 2.5Gbps cannot guaranteed (fall-back to 1000BASE-T).

Warning: Do not operate the standard PC7-FESTIVAL in systems with a 64-bit CompactPCI® backplane. The J2/P2 pin assignment of a 64-bit CPCI backplane differs substantially from a CompactPCI® PlusIO backplane, which will result in an overvoltage or short circuit situation on several pins, causing permanent damage to the PC7-FESTIVAL. For use together with a 64-bit CompactPCI® classic backplane, special PC7-FESTIVAL versions are available on customer request, however supporting only 32-bit peripheral cards. The use of 64-bit CompactPCI® classic peripheral boards may cause problems.

J2	A	B	C	D	E
22	*GA4* [2]	*GA3* [2]	*GA2* [2]	*GA1* [2]	*GA0* [2]
21	CLK6	GND	*2_ETH_B+*	*1_ETH_D+*	*1_ETH_B+*
20	CLK5	GND	*2_ETH_B-*	*1_ETH_D-*	*1_ETH_B-*
19	GND	GND	*2_ETH_A+*	*1_ETH_C+*	*1_ETH_A+*
18	*2_ETH_D+*	*2_ETH_C+*	*2_ETH_A-*	*1_ETH_C-*	*1_ETH_A-*
17	*2_ETH_D-*	*2_ETH_C-*	PRST# RST# [7]	REQ6# [1]	GNT6#
16	4_PE_CLK-	2_PE_CLK+	DEG# [1] [4]	GND	*reserved* [2]
15	4_PE_CLK+	2_PE_CLK-	FAL# [1] (PSON#) [6]	REQ5# [1]	GNT5#
14	3_PE_CLK-	1_PE_CLK+	4_PE_CLKE#	PPS [5] *SATA_SCL* [4]	*reserved* [2]
13	3_PE_CLK+	1_PE_CLK-	3_PE_CLKE#	PPM [5] *SATA_SDO* [4]	SATA_SL [4]
12	4_PE_RX00+	1_PE_CLKE#	2_PE_CLKE#	SATA_SDI [4]	4_SATA_RX+
11	4_PE_RX00-	4_PE_TX00+	4_USB2+	4_SATA_TX+	4_SATA_RX-
10	3_PE_RX00+	4_PE_TX00-	4_USB2-	4_SATA_TX-	3_SATA_RX+
9	3_PE_RX00-	3_PE_TX00+	3_USB2+	3_SATA_TX+	3_SATA_RX-
8	2_PE_RX00+	3_PE_TX00-	3_USB2-	3_SATA_TX-	2_SATA_RX+
7	2_PE_RX00-	2_PE_TX00+	2_USB2+	2_SATA_TX+	2_SATA_RX-
6	1_PE_RX00+	2_PE_TX00-	2_USB2-	2_SATA_TX-	1_SATA_RX+
5	1_PE_RX00-	1_PE_TX00+	1_USB2+	1_SATA_TX+	1_SATA_RX-
4	V(I/O)	1_PE_TX00-	1_USB2-	1_SATA_TX-	*reserved* [2]
3	CLK4	GND	GNT3#	REQ4# [1]	GNT4#
2	CLK2	CLK3	SYSEN# [3]	GNT2#	REQ3# [1]
1	CLK1	GND	REQ1# [1]	GNT1#	REQ2# [1]

signals marked grey/italic are not connected

The PC7-FESTIVAL does not provide backplane Ethernet by on-board controllers. As an *option*, the CPU card can be combined as an assembly with the *P82-GBE* low profile mezzanine module, which is populated with two I226-IT Ethernet controllers for 2.5GbE (4-speed, 10/100/1G/2.5G). By means of the mezzanine connector GBE these ports are wired from the P82 module to the carrier board backplane connector J2. The 2.5GBASE-T mode is not specified by the CompactPCI® PlusIO Specification. Where not applicable, the I226 controllers fall back to lower speeds by autonegotiation.

1) Various PCI control signals pulled up with 1kOhm to V(I/O). This resistor value is specified for +5V V(I/O) but works as well with +3.3V V(I/O) under all environments which have been tested by EKF. On request, 2.7kOhm P/U resistors can be stuffed.

2) GA pins and some other signals are not connected

3) SYSEN# is pulled up with 10kOhm to +3.3V

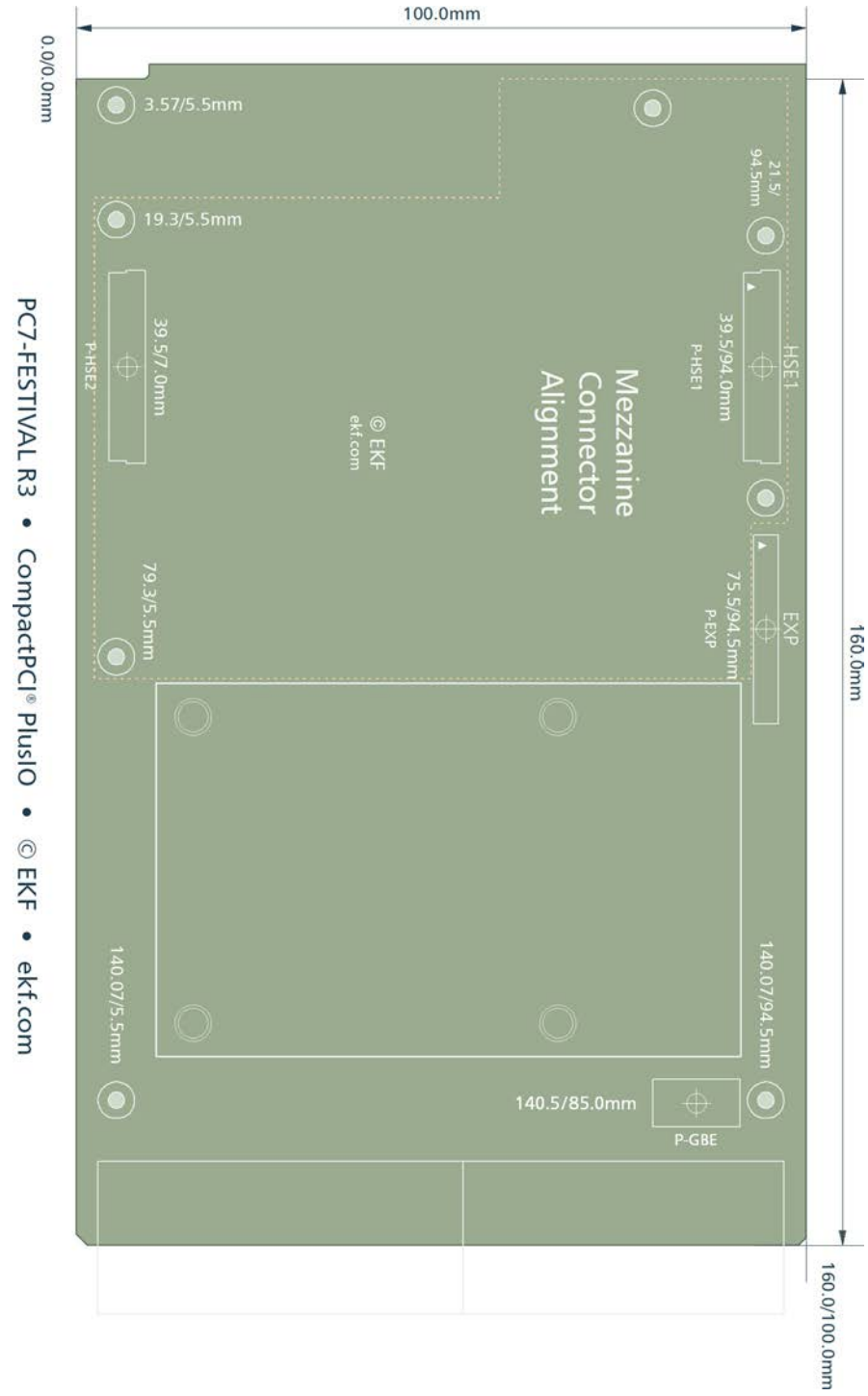
4) Signals terminated by P/U resistors, but not in use

5) PPS (pulse per second) and PPM (pulse per minute) as defined by IEEE 1588. These signals are derived from NIC1 (I210IT), and must be enabled by GPIO27 of the APL-I SoC, since this feature is EKF proprietary. According to the CompactPCI® Serial specification the SGPIO pins (i.e. PPM/PPS when enabled) are distributed via the CompactPCI® Serial backplane, and therefore can be used on a suitable peripheral card for triggering events. If a CompactPCI® Serial peripheral card makes use of the SGPIO sideband signals, the PPS/PPM signals should be disabled on the PC7-FESTIVAL.

6) As an exclusive stuffing option J2-C15 can be utilised as PSON# output

7) PRST# is pulled up with 1kOhm to +3.3V. This is normally an input, for optional connection to a push button (manual reset actuator). As an option, this pin may be reconfigured as RST# output (platform reset). This will be required for applications which address PCI Express® peripheral devices only via the rear I/O backplane connector J2, e.g. RIO modules. A similar situation arises as result of an optional PC7-FESTIVAL stand-alone configuration, where the backplane connector J1 has been replaced by a +5V terminal block. While J1 is present, RST# would be available on pin J1 C5. Without J1 however, the RST# output must be derived from J2 C17 as an alternate. Hence, if J1 is not populated on the PC7-FESTIVAL, backplane slots which are based on PCI Express® (typically configured according to CompactPCI® Serial) must be connected to J2/P2 C17 as platform reset.

Mechanical Details



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